DIGITAL DATALOGGING SYSTEM

PART I

A thesis submitted
In partial fulfilment of the requirements
for the Degree of

MASTER OF TECHNOLOGY IN ELECTRICAL ENGINEERING

by

Prabhat Kumar Rastogi

to the
Department of Electrical Engineering
Indian Institute of Technology, Kanpur

August 1969

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S.N. Jayaramamurthy

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CERTIFICATE

CERTIFIED that this work on "Digital Data Logging System" has been carried out under my supervision and that it has not been submitted elsewhere for a degree.

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ABSTRACT

Two schemes of digital data logging for the analysis of fading phenomena on troposcatter links have been discussed. A system using an on-line recording on an Analog tape unit and an off-line transcribing on a Digital tape unit has been discussed in greater detail. The problems in data-reduction have been discussed and a method of packing data for a one year period has been suggested.

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CHAPTER I

SYSTEM DESIGN

1.1 Introduction

An experimental Troposcatter link is being set up between Nainital and Kanpur. In the initial phases of the research program, it is intended to gather fading statistics on this channel at 2000 MHz. Such data are not yet available for this region and the extracted parameters from the experimental data are expected to yield useful information for system design. With this in mind the need was felt for a Digital Data Logging System which could store the raw data on digital tape in a format compatible with the IBM - 1401. With the IBM 7044/1401 system available at this institute, it would form a very effective Data Reduction System.

1.2 Statistics of Fading

Weak persistent fields due to scattering from lower layers of atmosphere, called Troposphere, are observed beyond the horizon. The path loss, depends upon the frequency and the distance between the transmitter and the receiver. The field strength at the receiver is accompanied with continuous fluctuations called fades. Detailed experimental data on statistical distribution of fade durations and fading rates are sparse. Such data, as are available, are reasonably consistent as to the trend and order of magnitude but are not in good agreement on the shape of distribution[1].

Typically observed fading rate in Troposcatter channels range from 0.1 to 1.0 fades/second at 400 MHz., to 1 to 10 fades/second at 4000 MHz. In individual experiments, however, the fade rates may vary from these values by a factor of 10 in either direction.[1].

The entire fading spectrum is roughly subdivided into i) Fast fades ii) Slow fades iii) Very slow fades. Fast fading, which is believed to be due to multipath effects, has a Rayleigh distribution and its sampling time has been found to vary from 1-5 minutes[4]. Superimposed on fast fading is a slow fading which is believed to be due to the change of refractive index of atmosphere. The median of received signal over a long period of time, of the order of hours, is found to obey a Log Normal distribution i.e. the values measured in db appear to obey a Gaussian distribution[1]. Deviation from Rayleigh distribution in short term fading are also occasionally observed because of other mechanisms of propagation like 'Ducting' and nonstationarity

upper limit on the bandwidth of fading envelope is fixed by the maximum fading rate of interest. The strip chart recorders* used in other experiments[3]* have a time constant of upto .015 seconds and will therefore average out the frequency contents beyond 66 Hz. We fix our upper limit as 100 Hz. For slow fades only frequencies below 10 Hz. may be of interest.

Sampling time for short term statistics should be of the order of 1 minute to 5 minutes. For hourly variation samples should be taken every hour and for diurnal and seasonal variations for a period of at least one year.

Besides the long-term median path loss over the channel, median signal strength over a short time is governed by the depth of fades. The seasonal variations have a dynamic range of upto 40-50 db. The diurnal variation of hourly median is also about 20 db at the most.[1,3] The system should therefore be able to handle a dynamic range of at least 70 db.

1.4 A Scheme for Data Logging

Our aim was to design a Digital Data Logging System for radio data with specifications given in 1.3. The system should have an overall accuracy of 1% and should record data in a format compatible with IBM machines.

It is possible to design such a system using an Incremental digital tape recorder. It is a special type of digital tape unit, used where the data input is at a relatively slow rate and

cannot be presented in a synchronous manner. The tape unit is commanded to step ahead (increment) for each character to be recorded. In this way each character is equally and precisely spaced along the tape[5].

The salient design considerations in view of data specification of 1.3 are:

1. Signal bandwidth 100 Hz.
2. Signal dynamics range 70db.
   The receiver is followed by a logarithmic amplifier which compresses the dynamic range of 70 db to a linear range.
3. Sampling the analog data for a period of five minutes/hour for short term statistics for fades upto 10 Hz.

In addition, an IBM compatible tape requires:

1. a 7 bit tape character, of which the last bit should be an odd parity check over the character.
2. a character packing density of 200 characters per inch.
3. an End of Record gap of width ¾" on the tape.
4. an End of File gap, after a certain number of records, of width about 3¼".

Since we are interested in statistics of fast fades upto 100 Hz. and slow fades upto 10 Hz., two separate analog blocks should be taken, one for each statistics. For slow fades an analog block of 5 minutes duration as used in other experiments[1,4] gives satisfactory results. At a Nyquist rate of 20 samples/sec., it requires a data block of 6000 samples. Same sample size is used for fast fades, which

gives an analog data block of 30 seconds at a Nyquist rate of 200 samples/second. An overall accuracy of 1% requires at least 7 bit coding of sample values.

Commercial tape units are available and specifications of two such units are given below.

Kennedy 1406 Magnetic Tape Transport (Option T-10) :

Records data on $\frac{1}{2}$ inch magnetic tape in 7-channel NRZI IBM compatible code and format. Density 200 bits per inch. Recording speed 400 characters per second. Gapping speed : Inter Record Gap $<$ 200 ms; End of File gap $<$ 700 ms. Reel capacity -1200 feet.

Kennedy 1506 Magnetic Tape Transport (Option T-11):

Same as above. Rell capacity - 2400 feet.

A feasible system designed around the above tape units as shown in Figure 1.1.

The receiver output is fed to a logarithmic amplifier which can handle a dynamic range of 70 db. The output of the logarithmic amplifier is passed through two low pass filters, with cutoff frequencies 10 Hz. and 100 Hz. respectively. Output of any of the two filters can be selected through a 'Select' pulse. The output of the selected filter is sampled at a Nyquist rate and is coverted to an equivalent 7 bit binary word in the ADC. Since the tape unit has 7 channels of which one is for parity, each 7 bit binary word is split up into two tape characters. This is done in the format encoder.

Each character is written in synchronism with a 'Step' command. The system is under the control of a master clock which monitors the following operations:

1. It switches on the tape recorder for 6 minutes/every hour.
2. It takes 6000 samples at 200 samples/second and 6000 samples at 20 samples/second.
3. Selects the proper filter for each sampling block.
4. Gives out two step commands for each sampling pulse.
5. Provides an Inter Record Gap after the first sampling block of 6000 pulses and an End of File gap after the second sampling block of 6000 pulses.
6. Stops the tape transport.
7. Initiates a new cycle after an hour.

The system thus operates on-line under the control of a clock. On a 1200 feet tape, it is possible to record uninterrupted data for five days and on a 2400 feet tape for ten days.

Due to the non-availability of an Incremental tape unit an alternative system is designed, using the available Honeywell 8107 analog tape unit and Potter MT-36 digital tape unit. This system is described in the next section.

1.5 The Proposed Digital Data Logging System

This scheme of data logging (Figure 1.2), which forms the subject of this report, is built around the two available tape units, one analog and the other digital.

Honeywell Model 8107 is a commercially available seven channel instrument tape recorder. In this tape recorder data can be recorded simultaneously on all the channels. Channel 4 is normally used for wow and flutter compensation. Four record and playback speeds are available viz. $1^7/8$ ips, $3\frac{3}{4}$ ips, 15 ips and 30 ips. Of these $3\frac{3}{4}$ and 30 ips speeds have IRIG compatible operation. Allowable signal bands are 0-625 Hz. at $1^7/8$ ips and 0-10 KHz. at 30 ips. Simultaneous playback of any two channels is possible.

The digital tape unit is a seven channel Potter Model MT-36. It has a single speed (50 ips) tape transport. IBM compatible tapes can be written at a packing density of 200 bits per inch and by providing an odd parity check over each six bit character on the seventh channel. Mode of recording is NRZI, in which only a '1' causes a flux reversal.

1.5.1 Block Diagram

Block diagram of the system is given in Figure 1.2. The ON-LINE SYSTEM operates under the control of a 50 Hz. mains controlled block. Timing and switching logic switches on the analog tape unit for six minutes every hour in the record mode at $1^7/8$ ips. During this time the output of logarithmic amplifier, passed through a signal conditioner is recorded on one of the data channels and a timing signal is recorded in parallel on an auxiliary timing channel. Signal conditioning provides level compatibility between the logarithmic amplifier and the tape unit and incorporates a 100 Hz. low pass filter.

In the OFF-LINE SYSTEM the analog tape unit operates in the playback mode at 30 ips and the digital tape unit in the record mode at 50 ips. The output of the timing channel enables the slave clock system to operate by gating the 1MHz. oscillator output. The output of the data channel is subjected to a signal conditioning to provide level compatibility with the ADC and is band limited to 1600 Hz., or 160 Hz. as desired. ADC is a ramp type seven bit encoder. Each seven bit word is split up into two six bit characters in the format encoder. The format encoder also generates an odd parity over each character. The characters are gated in succession and at a 10 KHz. rate and are written on digital tape through tape drivers. Timing for the operations is controlled through a 'Timing and Control Logic'. Control logic also provides for Inter Record Gap after every 10,000 characters and inhibits the 1MHz. clock after 20 such records are written. This corresponds to a real time of 320 seconds for analog data.

We may recall that the maximum frequency of interest in the fading envelope is 100 Hz. and for a short term statistics it may be necessary to record it for 5 to 6 minutes. The Nyquist rate for this signal should be 200 Hz. For an overall accuracy of 1% a 7 bit coding of analog data is desirable. This would need 2 characters per sample on the digital tape unit. Tape speed of 50 ips and bit packing density of 200 bits per inch fix up the sampling rate at 5000 samples per second. This is much in excess of the figure 200 Hz. quoted above. The analog tape unit can, however, be made to provide a time compression of upto 16 by recording the analog data at $1^7/8$ ips and playing it back at 30 ips. The significant frequency components are now upto 1600 Hz., for which

which the Nyquist rate is 3200 Hz. A higher sampling rate of 5000 Hz. would check any aliasing errors.

Following calculations provide a check on feasibility of the system:

Analog tape length	=	3600 feet
Digital tape length	=	2400 feet
Analog recording speed	=	$1\,^7/8$ ips.
Analog playback speed	=	30 ips.
Digital recording speed	=	50 ips.
Length of each analog tape consumed per data block of six minutes at $1\,^7/8$ ips.	=	$\dfrac{6 \times 60 \times 1\,^7/8}{12}$ feet
	=	56.25 feet
Start-Stop gap	=	0.75 inch.
Total number of analog records that can be accommodated on one analog tape of length 3600 feet	$\doteq$	$\dfrac{3600}{56.25} \doteq 64$
Playback time per analog record at 30 ips.	=	$\dfrac{6 \times 60}{16}$ seconds
	=	22.5 seconds.
Length of digital tape consumed per analog record	=	$\dfrac{50 \times 22.5}{12}$ feet
	=	93.75 feet
Inter Record Gap	=	$\frac{3}{4}$ inch.

Total number of analog records which can be transcribed on digital tape $\doteq \dfrac{2400}{93.75} \doteq 25$

Total run time of the digital tape $= \dfrac{2400 \times 12}{50 \times 60} = 9.6$ minutes

Analog data for two days can be stored on one tape of 3600 feet. In less than ten minutes, the analog data for one complete day can be transcribed on to one digital tape. Note that this can be done during one of the lulls of the ON-LINE SYSTEM (54 minutes).

The digital tape prepared in the above operation contains redundant data. The following data reduction is therefore carried on it using IBM 1401 computer.

i) Fast fading data : In 1.3 only 6000 samples collected over a period of 30 seconds were used for obtaining statistical distribution of fast fades. In the present case, however, almost the entire analog data block is transcribed on the digital tape. We need therefore retain only 2 records per file which corresponds to 32 seconds of real time. Furthermore, this can be packed at a high packing density of 800 bits per inch. Then since the bit packing density is four times and we are retaining only one tenth of the recorded information, each tape of length 2400 feet can keep a record of data collected over 40 days.

ii) Short term statistics: As in 1.3 for a short term statistics over a period of 4 to 5 minutes, frequency components upto 10 Hz. only should be retained. It is then possible to throw away the

redundant data by retaining the alue of every tenth sample. If this data reduction is carried on the intermediate tape, prepared through a 1600 Hz. filter, there will be errors due to aliasing. A separate intermediate tape should therefore be made through a 160 Hz. filter from which two consecutive characters corresponding to every tenth sample is stored on another tape at 800 bits per inch. Here also, since the packing density is four times and only one tenth of the original data is retained, a record of 40 days can be kept on one digital tape of length 2400 feet.

The fading data for one complete year can thus be stored on 20 digital tapes. This figure is quite reasonable. Retaining the data in this reduced form may prove to be of use later on during the program.

CHAPTER II

ON-LINE SYSTEM

2.1 Introduction

In this system, the output of the logarithmic amplifier is first passed through a signal conditioner and then recorded for six minutes every hour on one of the data channels of the analog tape unit. The digital clock from which the timing and switching logic is derived, uses 50 Hz. mains frequency as its reference. A timing signal, which is a pulse train with pulses of width six minutes and duty ratio 0.1 is generated from the digital clock. This signal is used to switch on the analog tape unit and maintain it in recording mode. During this period, the analog signal is recorded on Channel 1 while the timing signal is recorded on Channel 2. During playback, the latter generates a starting pulse for the slave clock that is used in the off-line system.

2.2 Signal Conditioning

Signal conditioning provides level compatibility between the logarithmic amplifier and the tape unit. It incorporates a 100 Hz. low pass filter, as frequencies higher than 100 Hz. are of no interest. (Figure 2.2)

A reference voltage V_R, which is needed for the calibration of the analog tape unit is also provided here. If the recorder is calibrated for 'V' volts, an input signal of $\pm$ V volts gives an output of $\pm$ 2 volts during playback. The transfer characteristic of the tape

unit calibrated for V_R volts is shown in Figure 2.3.

2.3 On-Line Analog Recording

The Honeywell 8107 tape recorder used in this system is primarily meant for manual operation. This recorder can be kept in recording mode by depressing the 'POWER', 'RECORD' and 'DRIVE R/P' buttons in that order, keeping the 'RECORD' button pressed while depressing 'DRIVE R/P' button. Alternatively the same end may be achieved by feeding mains supply to the tape unit while keeping the 'POWER' button in the 'ON' position and both 'RECORD' and 'DRIVE R/P' buttons firmly depressed.

The 'POWER' button can be permanently kept in the 'ON' position. The 'RECORD' and 'DRIVE R/P' buttons are held depressed by a mechanical lever. In this mode, the timing signal is used to drive a relay which feeds mains supply to the tape recorder so that the recorder automatically goes into the recording mode for a period of six minutes every hour. The analog signal and timing signal are recorded on Channels 1 and 2 respectively. (Figure 2.4)

2.4 Generation of the Timing Signal

The timing signal is generated by a digital clock which uses 50 Hz. mains frequency as its reference. To generate a 50 pps pulse train, the mains voltage (220 V/50 Hz.) is fed to a schmitt trigger through a step-down transformer. This frequency is counted down by a chain of counters to generate waveforms A and B, as shown in

Figure 2.5.a, with periods of 60 minutes and six minutes respectively on shaping these waveforms, signals C and D are obtained (Figure 2.6). The waveform C is used to set a flipflop FF1 'ON' and the waveform D is applied to the 'CLEAR DIRECT' terminal. The 'timing signal' (F) is obtained at the output of the flipflop FF1. (Figure 2.5b) A small delay is introduced in waveform C to prevent the simultaneous occurrence of pulses on both Trigger and Clear terminals of the flipflop.

2.5 Circuit Details

2.5.1 Counters

Motorola MRTL devices are used as building blocks in this system. A count down of N can be achieved using (n/2) MC890P (Dual J.K. flipflop) modules, where $2^n \geq N$.

The circuit diagram (Figure 2.7) illustrates the realisation of a decade counter (N=10) using MRTL modules.

The coincidence of Q_8 and Q_2 is detected by 'NOR'ing $\bar{Q}_8$ and $\bar{Q}_2$. This output is 'OR'ed with an 'External Reset' pulse by using two 'NOR' gates as shown and is used to clear the counter chain. The MC824P used in this circuit is a Quad - 2 input NOR gate for positive logic.

counters. In some places, Fairchild CuL 958 (which is a decade counter module) is used to save space.

A count down of 9 is realised in the same way by using the outputs Q_8 and Q_1 instead of Q_8 and Q_2 as in the previous case.

2.5.2 Delay Generation

The J.K. flipflop (MC890P), if connected as shown in Figure 2.8, behaves as a Monostable Multivibrator. This circuit is used to provide the necessary delay for the waveform C. The delay T introduced is proportional to RC.

2.5.3 Relay Drivers

The timing signal is used to drive a relay, which controls the application of mains supply to the analog tape unit. A relay with DPDT contacts with contact rating exceeding 1 ampere is required. The coil current must be small enough to be driven by a transistor. The IEC 'SOUDAMINI' relay conforms to the specifications and is used in the circuit as shown in Figure 2.9. A diode is used to clamp the initial voltage transients to the supply voltage. The capacitors across the contacts are used to prevent damage of contacts because of the inductive load.

The timing signal is passed through a buffer amplifier and is recorded on Channel 2 to provide the starting pulse for the slave clock during playback.

CHAPTER III

DATA FLOW IN THE OFF-LINE SYSTEM

3.1 Introduction

The data flow in the OFF-LINE SYSTEM is shown in Figure 3.1. Output of the analog tape unit is subjected to a signal conditioning which involves:

1. attenuation of ± 2V output to a range 0 to + 1.92 V as required by the ADC. This obviously involves a d.c. biasing, which is taken care of in the 'Sample and Hold' circuit.
2. appropriate filtering to limit base band. The base band is limited to 1600 Hz. if the intermediate tape is prepared for fast fading data. For 'short term statistics' it is limited to 160 Hz.

The 'Sample and Hold' circuit adds the required d.c. bias to avoid any negative excursions of signal, takes an almost instantaneous sample of 15-20 usec duration and holds it as a d.c. level while the conversion proceeds in the ADC.

The ADC is a modified precision ramp type convertor in which no reference voltage is used. It converts the sample values to an equivalent binary number. After conversion this number is transferred to a 'BUFFER' through 'AND' gates, leaving the ADC free for the next sample.

Format encoder splits up the seven bit encoded sample into two six bit characters with the option of a '1' or '0' in remaining five positions and generates an odd parity over these two characters.

Output characters of the format encoder are gated at a 10 KHz. rate with Write 1 and Write 2 pulses and are 'OR'ed, bit for bit, through seven 'OR' gates as shown in Figure 3.1.

The 'OR' outputs drive seven tape drivers for writing on the digital tape unit.

Timing operations are all in synchronism with the 1 MHz. slave clock. The generation of timing pulses is discussed in Chapter IV.

3.2 Sample and Hold Circuit

When the analog voltage changes rapidly during the conversion period of ADC, the converter settles on a value that does not equal the input at either the start or the finish of the conversion. Instead, it represents merely the value of the input at some undefined period during the conversion. If the change in the value of data during the coding interval exceeds the value of the least significant bit in the binary word, an output with error may result. The solution is to strobe the analog input very briefly (instantaneous sample) and hold this value as a d.c. level during the conversion period. The strobed value then represents the correct voltage for some well defined moment

The basic 'Sample and Hold' circuit, in an ideal case has the configuration shown in Figure 3.2a. S_1 and S_2 are ideal analog switches (zero 'ON' resistance, infinite 'OFF' resistance and zero offset voltage in the 'ON' state) and C is a loss free capacitor. Ideally S_1 is closed for an arbitrarily short period and C charges instantaneously to the value of the input voltage and retains it till S_2 closes. An ideal 'Sample and Hold' has neither 'offset' nor 'storage' errors. These creep in a practical circuit (Figure 3.2b) due to:

1) finite source resistance, Rs.
2) finite 'ON' and 'OFF' resistances of analog switches (r_{on} and r_{off} respectively)
3) offset v_o in analog switches and input and output buffer stages.
4) self leakage resistance (r_1) of the capacitor and finite input impedence r_{in} of other circuits loading the 'Sample and Hold' circuit.

To minimize the offset and storage errors:

1) a low output impedance buffer should be used at the input
2) a high input impedance buffer should be used at the output
3) JFETs or MOSFETs should be used as analog switches and
4) Ceramic or Mica condenser should be used as temporary storage device.

In this particular case, total offset and storage errors of $\pm$ 5 mV can be tolerated ($\pm \frac{1}{4}$ least significant bit in the binary word). The schematic of the circuit is shown in Figure 3.2c. Q_1 and Q_2 are n - channel JFETs and A_1 and A_2 are unity gain buffers. The sample one-shot turns on Q_1 for a short duration, about 3 to 4 times the time constant of the charging circuit while the hold one-shot keeps Q_2 cutoff during the hold period. This particular use requires adding a d.c. level of +.96 volts to the input to avoid any negative excursions of signal. A negative reference voltage of .96 volts is therefore added to the negative input of A_1. The complete circuit details are given in Figure 3.2d.

Input and output buffers are unity gain operational amplifiers MC1709CG, which are frequency compensated upto 500 KHz. The reference voltage of .96 volts is obtained from a Zener - emitter follower configuration shown in Figure 3.2e. CZ5 has a breakdown voltage in the transition range 4.5 - 6.0 volts and its temperature coefficient is very small. Emitter follower configuration serves to reduce the output impedance and puts a forward biased diode in series with the zener which further reduces the temperature coefficient of the combination. The n - channel JFETs require a negative excursion of -15V for complete cutoff. The one-shot modules in the system are realised using MOTOROLA MECL NOR gates with logical '0' level $\doteq$ 0.5V and logical '1' level = + 1.5V. To switch a negative voltage from these logical levels, 3 silicon diodes were placed in series which provide a drop of 1.8V. The logical '1' level in positive logic now becomes - 0.3V which is a logical '0' in negative logic and the

logical '0' level in positive logic becomes -1.3V which is a logical '1' in negative logic. These levels can switch a higher voltage of upto -30V. The overall effect of these two logical inversions is:

Logical '0' level (positive logic)	= + 0.5V	Logical '1' level (negative logic)	= - 0.2V
Logical '1' level (positive logic)	= + 1.5V	Logical '0' level (negative logic)	= - 15V

The output of the inverters can now drive the JEETs.

The circuit performance is now calculated in order to assess errors introduced in the holding operation.

r_{on}	, JEET 'ON' resistance	= 150
r_s	, Amplifier MC1709CG output resistance	= 150
C	, Storage capacitance	= .022uF
t_c	, Charging time constant = $(r_{on} + r_s)C$	= 6.6 us.

A sample pulse duration of about 20 us should therefore be used.

A simple and straightforward analysis shows that for a conversion time T, for storage errors to be less than the least significant bit in the binary word, the decay time constant in the hold mode should be t_d 2^n T where n is the binary word length and the count-up clock in the ADC is synchronized with the remaining timing operations.

For a 1 MHz. clock and a seven bit word, T = 128 us and t_d should be greater than 128 x 2^7 us = 16.4 ms.

For the circuit shown in Figure 3.3c:

r_{in} , input impedance of output buffer = 1 MΩ

r_{off} , off resistance of JFET = 10 MΩ

the decay time constant = $\frac{(r_{off} \parallel r_{in})}{2} \cdot C$

$= 10^6 \times .022 \times 10^{-6}$ sec

$=$ 22 ms.

Hence the decay would cause a storage error of less than the value of the least significant bit.

A switching transient is observed at the output of the circuit at the end of the hold period. This is of no consequence as the conversion is already over by this time and ADC contents transferred to the buffer.

Before the next cycle of operation the circuit should settle down to a zero output and to ensure this, the settling time $T_c \geqslant 4 \times t_o$ where t_o is the discharge time constant when the 'Hold' mode is removed.

$\therefore \quad t_o = C \times r_{on} = .022 \times 150 = 3.3$ us

$T_c = 30$ us

Therefore before the next cycle the capacitor C discharges completely.

To reduce amplifier offsets and drifts the feedback resistances and the input resistances are matched to within 0.05%.

3.3 Analog to Digital Converter (ADC)

The Analog to Digital Converter encodes the sample value to an equivalent binary word with an accuracy determined by the value of the least significant.bit. The basic system (Figure 3.3a) shows the major components of an ADC. The Reference determines the voltage levels of the ladder switches driving the 'Resistor Ladder Network'. This ladder forms a digitally generated ramp at its output that is compared to the analog input in the 'Comparator'. The comparator output tells the logic either that the conversion (Counting-Up) must continue or that the voltages are equal within prespecified limits and the binary coded voltage should be read out of the 'Counter'.

In this particular design, the need for analog switches was avoided on the basis of following observations:

1) The logical '1' and '0' levels of MC890P flipflops have a 5% tolerance with the 'Q' output loaded by the 'Toggle' terminal of another flipflop and '$\overline{Q}$' open. Loading the '$\overline{Q}$' output with a unit fan in causes a change of at the most ± 5 mV in the 'Q' output.

2) The loaded 'Q' output remains within ± 5 mV for a ± 10°C change in the environmental conditions.

3) Reasonably good analog switches, JFETs, cause a problem with this circuit configuration. Only n-channel FETs are available which require a 0 to -15 V gate excursion for switching. To switch this voltage from MRTL modules,

involves changing the positive level logic to negative level logic through diodes and then switching a pnp transistor from 0 to -15 V. This voltage would then operate the JFET. The delay involved in the process is of the order of microseconds, comparable to the clock time.

It was therefore decided to sum the outputs of the flip-flops in the counter through a binary ladder network and operational amplifier and subtract from it the weighted sum of all the '0' levels. The resistances in the ladder have a 5% lattitude to take care of the 5% tolerance of the '1' level of loaded 'Q' output mentioned above. Following a calibration procedure described later in this section a 15 mV ± 1 mV step size was obtained over a dynamic range of 0 to 1.8 V. The offset registered over a 6 hour run was ± 3 mV.

Since these figures meet the desired requirements for the ADC in the data logging system, the design shown in Figure 3.2b was finally adopted. A typical calibration curve is shown in Figure 3.2c.

For calibrating the ADC, it is removed from the system and instead of 1 MHz. clock, pulses from a monopulse generator are used for counting up. A monopulse generator gives out a narrow pulse on pressing a switch. The most significant bit offset is adjusted so that $Q_7 = 1.25$ V. The output of the ladder summing network is now monitored with a digital voltmeter. R_7 is set to get an output of 960 mV with only Q_7 on. Then R_6 is adjusted to get an output of 480 mV with only Q_6 on. This process is continued till R_1. Now the offset is

annulled by changing the 'zero offset'. The process is reiterated till it converges.

3.4 Transfer to Buffer

Conversion in the ADC takes a maximum of 128 us. The 7 bit binary word is split up into two tape characters, which are written on tape at 10,000 characters/second. Writing two consecutive characters on tape requires minimum 100 us. The 200–128 = 72 us interval available, before next conversion cycle in the ADC, is insufficient to write the value of one sample. A temporary storage is therefore needed.

Contents of the ADC are transferred to a 7-bit buffer through 7 gates and the ADC is reset for the next cycle of operations. Since the 'Q' output of the flip-flops in the ADC are used as ladder inputs, each '$\overline{Q}$' output is 'NOR'ed with the complement of 'Transfer' pulse and the output is used to trigger a cleared flipflop. All flipflops of the buffer are cleared before the next 'transfer' operation.

3.5 Fortmat Encoding

Format encoding involves:

i) splitting the 7-bit binary word from the 'BUFFER' to two tape characters each of 6 bits. This may need 5 dummy bits which can be '1' or '0'.

ii) generating odd parity over the two tape characters.

The dummy bits can be supplied in any desired positions by patching up a card. (Figure 3.5) This permits some flexibility in the software operations.

3.5.1 Parity Generation

IBM compatibility requires that corresponding to each character of six bits, an odd parity be written on the seventh channel. The basic parity checking circuit is an 'EXCLUSIVE OR' gate in which the output is '1' iff one of the two inputs is '1'. Thus the output of an 'EXCLUSIVE OR' gives an even parity over a two bit character. By arranging 'EXCLUSIVE OR' gates in an inverted tree structure it is possible to generate parity over a character of more than two bits. A parity generating structure for a six bit character is given in Figure (3.6a), its output $Y = S^{6}_{1,3,5}$ is an even parity over the character. Odd parity can be obtained by complementing Y.

This structure is particularly amenable to integerated circuit implementation. Each 'EXCLUSIVE OR' and its complement can be obtained by pin interconnections of 2-input Quad 'NOR' gates. Complement of the six bits of a character is generated through a hex-inverter.

3.6 Writing Logic

The two 7 bit characters available at the output of the format encoder are to be written consecutively on the tape at a rate of 10,000 characters/second. The two characters are gated with Write 1 and Write 2 pulses and are then 'OR'ed as shown in Figure 3.7.

3.7 Tape Drivers

In the NRZI recording method used for IBM compatible tapes, a '1' is recorded by reversing the magnetization on the tape.

The tape driver circuit is shown in Figure 3.8. A current of 38 mA through tape head coil is required to saturate the magnetic material on tape. The tape head coil is provided with a centre tap. The centre tap is connected to a 38 mA current source. Normally, one end is connected to ground directly and the other, through a high resistance. The direction of current through tape head coil, and hence the magnetization on tape, can be reversed by commutating the end connections. The commutating action can be obtained by connecting the opposite ends of tape head coil to 'Q' and '$\overline{Q}$' outputs of flipflop. A '1' applied to the toggle terminal of the flipflop reverses the magnetization on tape.

A MOTOROLA MRTL flipflop does not have a current sinking capacity of 38 mA. A two stage buffer is, therefore, put in series with each of 'Q' and '$\overline{Q}$' outputs. Diodes D_1 and D_2 quench the switching transients.

IBM format also requires a longitudinal parity check, which is an even parity check, over each channel. This is obtained by clearing all the driver flipflops, 300 us after the last character is written in the record.

A $\frac{3}{4}$ inch Inter Record Gap is provided after a record of about 10,000 characters. This corresponds to a 15 ms interval at a tape speed of 50 ips, during which time a 'Write Disable' pulse inhibits the system operation. This means that after 10,000 characters, subsequent records will contain only 9850 characters while 150 characters (75 samples) are lost. This is quite unavoidable. A few cycles in the original signal are thus lost.

CHAPTER IV

CONTROL FLOW IN THE OFF-LINE SYSTEM

4.1 Introduction

The timing for the OFF-LINE SYSTEM is obtained from a crystal controlled digital clock. The starting of the clock is initiated by a 'START' pulse generated during playback of the timing channel. The digital clock is required to supply the following timing signals:

1) 1 MHz. count-up pulses to the ADC.

2) 10 KHz. pulses for the generation of control pulses to the writing circuits.

3) 5 KHz. pulses for generating the sampling pulses to the 'Sample and Hold' circuit.

4) 1 Hz. control pulses for the generation of 'Inter Record Gap' and 'Longitudinal Parity' over a record.

After a predetermined number of samples are written from an analog data block on to the digital tape, the digital clock is stopped. It is initiated again by the next 'START' pulse indicating the beginning of the next analog data block. This ensures the recording of equal number of samples from each block.

Each analog data block is recorded on a single file consisting of 20 records. Each record contains nearly 10,000 characters. A longitudinal parity check character, which is an even

parity check on each channel and is obtained by resetting the tape driver flipflops, must appear after 300 usec have elapsed since writing the last character. A $\frac{3}{4}$ inch Inter Record Gap provided in between records corresponds to 15 ms at a tape speed of 50 ips.

A day's data accumulated on the analog tape is played back at the end of the day and is converted and recorded on digital tape under the control of a digital clock. The digital clock operates for less than 10 minutes every day.

4.2 Length of File

There is no file length restriction in most of the IBM machines except that the file length should not exceed that of one tape. It is then logical to write one complete data block (written for 6 minutes in an hour in real time) as one file. After the START pulse is obtained, the data can be sampled for 20 seconds and is converted into digital form. This provides 200,000 characters in a file and corresponds to 320 seconds in real time.

4.3 Length of Record

Again there is no restriction on the length of record except that it should not exceed the memory capacity of the computer being used to process the data under consideration. As the computer being used to process the data (in this case IBM 1401) has a memory capacity of 16,000 characters, the length of the record can be fixed as nearly 10,000 characters.

4.4 Inter Record Gap (IRG)

Each record should be separated from its predecessor by a $\frac{3}{4}$ inch IRG to enable the starting and stopping of tapes in between records during computation. The lower limit on the IRG is 0.697 inch for all tape units and is extremely critical. The upper limit is 0.92 inch for IBM tape model 729-IV and V and is 0.8075 inch for model 729-II.

4.5 Generation of 'START' pulse

The output of the timing channel during playback is fed into a low pass filter followed by a schmitt trigger as shown in Figure 4.2. The timing waveform is recorded simultaneously with the data block on a parallel channel. During playback, the timing waveform causes gradual building of voltage at the output of the low pass filter, indicating the beginning of the data block. When the output reaches a predetermined level, the schmitt trigger switches 'ON'. The output of the schmitt trigger is fed into a wave shaping network to generate 'START' pulse. The waveshaping network consists of a differentiator and a buffer amplifier. The low pass filter helps in curbing the sharp noise spikes that may appear in the signal read from the tape, which would otherwise switch the schmitt trigger.

4.6 The Digital Clock

The block diagram of the digital clock is shown in Figure 4.3. The crystal controlled astable multivibrator generates a 1 MHz. pulse train. This is used as a standard source and is counted down to generate the required timing pulses.

The flipflop FF1 is cleared with the occurrence of the 'START' pulse. The 'Q' output of the flipflop now allows the 1 MHz. pulses through the 'NOR' gate into the chain of counters. The 1 MHz., 10 KHz., 5 KHz. and 1 Hz. signals are tapped at A, B, C and D points respectively as indicated in Figure 4.3. After 10,000 samples are recorded, the last decade counter overflows triggering the flipflop FF1. The output of the flipflop now prevents the entry of pulses into the counter chain. The system remains in a quiescent condition until the arrival of the next 'START' pulse. This 'START' pulse is also used to reset the counter chain.

4.7 Circuit Description

4.7.1 Crystal Oscillator

The circuit shown in Figure 4.5 is basically an emitter coupled astable multivibrator. The circuit comprises two 'NOR' gates of MC824P (QUAD - 2 input - gate) and operates like any conventional astable multivibrator except that the output of Q_2 is used to excite the crystal instead of charging a capacitor. Because of this the circuit is forced to oscillate at the crystal frequency. The silicon diodes connected at the output bring the base of the waveform to the ground level as shown in Figure 4.5.

4.7.2 Counter Chain

The basic decade counter module used in the counter chain was described in Chapter II.

4.7.3 Generation of Inter Record Gap

The 1 Hz. waveform D is passed through a circuit with a delay of 15 ms to generate a 'Write Disable' signal. The 'Write Enable' signal, obtained by inverting the 'Write Disable' signal is 'AND'ed with the 10 KHz. timing pulses, thus blanking these pulses for 15 ms during which time the Inter Record Gap is provided as shown in Figure 4.7.

4.7.4 Longitudinal Parity Generation

A longitudinal parity check character is to be written 300 usec after the last character is written in a record. The waveform D is passed through a 300 usec delay circuit and is used to reset the tape driver flipflops, when the longitudinal parity is recorded on tape.

CHAPTER V

PACKING

1 Introduction

Separate tapes can be prepared for the analysis of st fades, slow fades and very slow fades by including ppropriate filters in the Data Logging System. We may recall at each sample is coded into seven bits, as there are 128 antization levels, and are recorded as two consecutive characters the tape, at a low density. During the 'packing' operation, e redundant characters that are present in the record are rejected d the rest of the information is recorded at high density on a ster tape. The operation is performed using an IBM 1401 computer.

In some cases only 64 quantization levels would suffice equiring only six information bits per sample, which can be written s one character. In such a case, twice as much information can be tored on a tape.

The format in which information is stored on the tape repared by the Data Logging System is shown in Figure 5.1.

.2 Fast Fades

In the case of fast fades, the information is needed or only a short duration (of the order of thirty seconds) in real ime. The first two records in each file, comprising of 19,850

characters, is read into computer core memory. 9000 characters from each record are selected and written as a separate record on a master tape at 800 bits per inch. This corresponds to two records of 14.4 seconds each, in real time as shown in Figure 5.2. These two records cannot be merged into the same record as some samples are missing. If a continuous block of data is needed for calculation, then only the first record may be used. Nevertheless, both the records can be stored on the tape.

It may be shown that a master tape of 2400 feet can store the data of fifty days on it. If it is decided to use 64 quantization levels only, the second character in each sample is discarded in which case a master tape of 2400 feet can store 100 days' data. The second character can be identified by testing the pattern ofthe dummy bits over about ten alternate characters.

5.3 Slow Fades

There are many redundant samples as the sampling frequency is 10 times that of the required frequency. Of every ten samples one sample may be retained that is, two consecutive characters may be stored for every 20 characters. The non-redundant characters from each file are accumulated in a separate portion of the memory. The first 18,000 characters are written as one single record on the master tape. This number satisfies the requirement that the number of characters in a record need be a multiple of six

for the IBM 7044 computer, and corresponds to 288 seconds of data in real time. Here also master tape can store 50 days' data. Alternate characters are discarded if only six bits per samplc are needed retaining all first characters in each sample.

5.4 Very Slow Fades

Here one sample out of every 100 samples is selected and recorded at high density, as in the previous case. A master tape can store a complete year's data on it.

CHAPTER VI

SYSTEM LAY- OUT

6.1 Introduction

The Digital Data Logging System, described in the previous chapters, is realised using Motorola MRTL Integrated Circuit Modules. The lay-out of the complete system is shown in Figure 6.1 a. The ON-LINE SYSTEM and the digital clock for the OFF-LINE SYSTEM are housed in bin B. Bin A accommodates the rest of the OFF-LINE SYSTEM. The analog tape unit is mounted on the rack as shown in Figure 6.1.

6.2 Lay-out of the ON-LINE SYSTEM

The lay-out of the ON-LINE SYSTEM is shown in Figure 6.2. The input to the system is taken from a 220V/4.5V step down transformer. Using this input, the 'timing signal' is generated in two cards, C2.1 and C2.2.The relay driver circuit and the buffer amplifier circuit are located on C1.3. The relay and the step-down transformer are mounted in a small box.

The card, C1.1, is mounted in the position B-14 in bin B. The circuit details of this card are shown in Figure 6.3. The input to the schmitt trigger is given at the terminals J and D. The output of the schmitt trigger is passed through an emitter follower and the generated 50 pps waveform is given to the

counter chain. The count down of 9 is achieved using 2 MC890P modulus and an MC824P module, interconnected as shown in Figure 6.3. The output is available at the pin C, which is connected to pin M of C1.2.

The card C1.2 contains circuits which derive their input from card C1.1 and generates the 'timing signal' at the pin F. The details of the card are shown in Figure 6.4. The input is passed through a flipflop (½ MC890P) and is fed into a chain of decade counters. Four Fairchild CuL 958 Integrated circuit modules are connected in series and the waveforms A and B are obtained at points shown in the diagram.

These waveforms are now connected to the toggle and clear terminals of a flipflop - ½MC890P - (as shown in Figure 6.3), when the 'timing signal' is generated at the 'Q' output of the flipflop. A small delay is introduced in one of the waveforms to prevent the simultaneous occurrence of pulses on both the toggle and clear terminals. The necessary delay is generated in a flipflop (½MC890P) when connected as a monostable multivibrator as described in Chapter II.

The card C1.3 contains the relay driver and the buffer amplifier. The relay is connected in the collector of a switching transistor and a current of 2.4 mA is switched when the 'timing signal' is in the 'ON' position operating the relay. Through the

double pole double throw contacts of the relay mains power is applied to the analog tape unit. The buffer amplifier consists of two inverters. The timing signal is passed through the buffer amplifier and is written on channel 2 of the analog tape unit.

6.3 Lay-out of the OFF-LINE SYSTEM

The lay-out of the digital clock for the OFF-LINE SYSTEM is shown in Figure 6.5. The crystal controlled oscillator is mounted on card c2.1. The counter chain is mounted on the next four cards. The sixth card contains the circuits for the generation of the delays to provide for the Inter Record Gap and the Longitudinal Parity check character over a record. The 'STARE' pulse is generated in the card C2.7.

The card C2.7 receives the input from the playback channel 2 of the analog tape unit. The low pass filter output gradually develops as the 'timing signal' is fed at its input. This output is fed to a schmitt trigger. The output of the schmitt trigger is differentiated and is passed through two 'NOR' gates when the 'START' pulses appear at the output.

The crystal oscillator circuit, which was described in Chapter IV, is mounted on card C2.1. The output is available at pin L which is fed into one of the inputs of the 'NOR' gate located on the card C2.2. The other input to the 'NOR' gate is taken from a

flipflop ($\frac{1}{2}$MC890P) as shown in the Figure 6.6. This flipflop receives its clearing signal from the 'START' pulse applied at pin Z and is set by the last decade counter in the counter chain. The binary and the last decade counter in the counter chain are housed in this card. The output of the 'NOR' gate is available at pin E which is fed into the counter chain.

Three dual-decade counter cards are connected in series to form a part of the counter chain. The decade counter circuit is discussed in Chapter II. The output of the sixth decade counter is fed into the binary located on the card C2.2, thus completing the loop as shown in Figure 6.5. The 1MHz., 10KHz., 5KHz. and 1Hz. signals are tapped at points A, B, C and D respectively.

The card C2.4 contains two delay circuits with delays 300 usec and 15 msec. The details of these circuits have been discussed in earlier chapters. The 1Hz. signal is fed to the input of these circuits. The 'Write Disable' signal is available at the output of the 15msec delay circuit. The complement of this signal is 'And'ed with the 10KHz. signal and is used to generate a control signal for the writing circuits.

The lay-out of the bin B is given in the table below:

Card Position	Card Number	Function
B_1	C2.1	Crystal oscillator
B_2	C2.2	Gating circuit
B_3	C2.3	Dual decade counter
B_4	C2.3	Dual decade counter
B_5	C2.3	Dual decade counter
B_6	C2.4	IRG, longitudinal parity generation
B_7	C2.5	'START' pulse generation
B_8	-	
B_9	-	
B_{10}	-	
B_{11}	-	
B_{12}	C1.3	Relay driver circuit
B_{13}	C1.2	Circuits for the generation of the 'timing signal'
B_{14}	C1.1	

Bin A houses the following circuits:

i) The Sample and Hold

ii) Logic to control timing operations of circuits in bin A.

iii) ADC and Ladder network

iv) Transfer to Buffer logic

v) Format encoder

vi) Gating and writing logic

vii) Tape drivers.

The lay-out of the bin A is given in the table below:

Card Position	Card Number	Function
A_1	C3.1	Sample and Hold
A_2	C3.2	Control logic
A_3	C3.3	ADC (7 bit)
A_4	C3.4	Ladder network
A_5	C3.5	Transfer to Buffer card
A_6	C3.6	Patch up card
A_7	C3.7	Parity check card
A_8	C3.7	Parity check card
A_9	C3.8	7 and gates

A_{10}	C3.8	7 and gates
A_{11}	C3.9	7 or gates
A_{12}	C3.10	4 tape drivers
A_{13}	C3.11	3 tape drivers
A_{14}		

The configuration of the OFF-LINE SYSTEM is shown in the Figure 6.8.

The analog signal is fed to card C3.1. (the Sample and Hold circuit). The timing operations are supplied through card C3.2. Output of the Sample and Hold drives the ADC. C3.3 and C3.4 constitute the complete ADC and the two cards are joined internally. The seven bit output of ADC is transferred to a seven bit buffer (card C3.5) at the end of conversion. Cards C3.6 and C3.7 split the seven bit word into two six bit tape characters, generate an off parity over each character. The two tape characters are 'AND'ed in two C3.8 cards and their output is 'OR'ed in C3.9. The outputs of the 'OR' gates operate the tape drivers, 4 on card C3.10 and three on C3.11.

In the Sample and Hold circuit (C3.1), unity gain buffers are MC1709CG High gain operational amplifiers, with proper

feedback. (Figure 6.9) Logic changing circuits, change the positive logic output (Logical '0' = .5V and Logical '1' = 1.8V) to a negative logic (Logical '0' = -.2V and Logical '1' = -15V). to drive the FET's. This involves dropping the positive level logic through three silicon diodes (CD22) and then switching a p-n-p transistor (2N995) across a -15V supply.

The control logic on card C3.2 (Figure 6.10a) accepts the 5KHz. basic timing signal from the slave clock generates pulses for sampling, holding, transferring to buffer and clearing the ADC. At the rising edge of the 5KHz. waveform, a trigger pulse is generated through differentiation and clipping, followed by 2 stage non-inverting buffer. This trigger pulse is fed simultaneously to three one-shots with periods 15 us, 170us and 127us respectively. 15us pulse is used for sampling and 170us for holding. After 127 us a 10us wide pulse is generated through an identical operation for transferring the ADC contents to the buffer. Another 10us wide pulse at the end of hold interval clears the ADC.

Each one-shot is realized through a Quad-2-input 'NOR' gate (MC824P) as shown in Figure 6.10b.

The ADC card, C3.3 uses MC1709CG operational amplifiers as summing amplifier and comparator. C3.4 is the ladder card and also contains the resistance for loading the MSB flipflop and an offset adjustment (Figure 6.11). All the resistance are

connected in series with 10% potentiometer for calibration. The $\overline{Q}$ outputs of the counter are available at the amphenol points for subsequence operations.

C3.5 contains the 'AND' gates and a seven bit buffers. (Figure 6.12) To derive the seven circuits two high fan out buffers are also provided on the same card. The transfer pulse is obtained from C3.2 and with its occurrence, the transfer is 'NOR'ed with $\overline{Q}$ outputs of C3.3 and the output triggers a flipflop.

C3.6 is a patch up card to split the seven bit (Figure 6.13) ADC word to two IBM compatible tape characters. The details of this card are mentioned in Chapter III. C3.7, the parity check cards, are used to generate an odd parity over each six bit tape character obtained from the patch card. It uses a Hex inverter MC884P and 5 Quad 'NOR' gates, MC824P. Each MC824P is interconnected to function as an 'EXCLUSIVE OR' gate.

The gating logic of A_9, A_{10} and A_{11} uses MRTL logic modules to achieve the 'AND'ed 'OR' functions. C3.8 has 7-AND gates, obtained by complementing the inputs through a Hex inverter MC889P and a 2 input 'NOR', and 'NOR'ing these with the complement of WRITE pulse. The complement of the WRITE pulse is obtained through a buffer $\frac{1}{2}$ MC889P for higher fan-out. The 'OR' function is achieved by complementing a 'NOR' output. Due to lack of pins on amphenol, one output point of C3.9 is internally connected to C3.10.

C3.10 and 3.11 have four and three tape drivers respectively. The outputs from C3.9 toggle flipflop on the driver cards. The Q and $\overline{Q}$ outputs of flipflops are buffered by a 'NOR' or a 'NOT' gate to provide a fan-out of 5 instead of 3 available from flipflop modules MC890P. The available current of 3.0mA can switch 38mA through tape head coils connected as collector load of a CIL 701 n-p-n transistor. The bit positions and parity output of format encoder are indicated in Figures 6.13 to 6.18.

CHAPTER VII

OPERATION MANUAL

7.1 Calibration of the Honeywell Tape Recorder (Model 8107)

To assure a high degree of accuracy and linearity at all times when recording or reproducing data signals, it is recommended that the following calibration procedure be followed just prior to each and every operation. When extreme accuracy and linearity is required, the recorder should be recalibrated before playback and any time the playback speed is changed.

7.1.1 General

a. Place the 30 ips/EXT center frequency filter card in the primary position (channels 1-4) and 1 7/8 ips/EXT center frequency filter card in the secondary position (channels 1-4) as shown in Figure 3-7 of the manual.

b. Set the speed selector to 30 ips.

c. Turn Function Selector to the OFF position and the press 'POWER' and 'RECORD' push buttons.

7.1.2 Compensation Discriminator

a. Set Channel Selector switch to C.

b. Turn Function Selector switch to ZERO P/B.

c. Adjust compensation zero screw for meter null.

d. Turn Function Selector to SENS P/B.

e. Adjust compensation gain control for meter null.

f. Repeat steps b through e.

7.1.3 Record Oscillators

a. Turn Function Selector switch to ZERO/REC

b. Place the probe 'R' (Figure 7.1) in one of the input channels and select that channels by the Channel Selector switch.

c. Set the switch SW1 in position 'P'.

d. Adjust the Record Oscillator center frequency zero screw for meter null.

e. Turn the Function Selector switch to SENS/REC

f. Put SW1 in position 'Q'

g. Adjust the Record Oscillator gain control for meter null.

h. Repeat steps b through g

j. Repeat steps a through h for all channels

7.1.4 Playback Discriminators

a. Turn Function Selector switch to ZERO P/B.

b. Adjust each Playback discriminator zero screw for meter null, setting the Channel Selector switch to the

respective channel position. (NOTE: Only two playback channels are available in the present model. Any one of the seven recorded channels can be reproduced on each playback channel as selected by the individual selector switches. The positions of these switches is immaterial during calibration).

c. Turn Function Selector switch to SENS P/B

d. Adjust each Playback discriminator gain control for meter null, setting the Channel Selector switch to the respective channel position.

e. Repeat steps a through d, then press the STOP pushbutton to remove RECORD condition. Turn Function Selector switch to OFF position.

7.2 On-Line Recording

Turn on the +3.6V and +15V supplies for the ON-LINE SYSTEM.

Zero the reel rotation counter of analog tape unit with minimum amount of tape wrapped on the take-up reel.

Press the 'POWER' pushbutton 'ON'

Press the mechanical lever to press the 'RECORD' and DRIVE R/P buttons firmly. (Make sure that the tape recorder goes into RECORD mode as soon as the

mains supply is given).

Place the power cable into the plug socket which receives the mains supply when the relay is 'ON'.

Press the 'RESET' button at a predetermined time of the day. (An electric clock may be used as reference and it is preferable to start the system at the beginning of an hour). The system goes into operation and starts recording the data every hour for six minutes.

7.3 Playback

At the end of 24 hours of recording, the analog data must be transcribed on to the digital tape.

Disconnect the recorder from the ON-LINE SYSTEM without disturbing its clock.

Note the reading of the reel location counter

Remove the mechanical lever

Rewind the tape to the beginning ofthe data block.

Select 30 ips speed.

Turn on the supplies for the OFF-LINE SYSTEM.

Check the crystal oscillator output.

Connect the inputs of the system to the output channels of the analog tape unit.

Plug the patch panel of the format encoder as desired (card C.3.6)

Mount a tape on the digital tape recorder. Make sure there is a ring on the back of the tape reel to record. Permit light will go on.

Turn tape deck ON. Turn left switch to MANUAL and press white button LOAD POINT. This will move the tape forward to the silver indication which marks the beginning of recorded information.

Connect the system output terminals to the input terminals of the digital tape.unit.

Include the appropriate filter in the system.

Both the tape digital tape recorders are putinto operation simultaneously, the analog tape unit on PLAYBACK mode and the digital tape unit in manual 'Record' mode.

The transcription of the data takes place automatically. At the end of the analog data as indicated by the reel location counter, both the tape units are stopped. The digital tape is rewound and is ready for processing. The analog tape is also rewound and is included in the ON-LINE SYSTEM as described earlier.

The whole operation should not take more than 30 minutes and must be performed in the lull period of the system.

7.4 ADC Calibration

The ADC uses only one reference voltage of 0.96V in the Sample and Hold circuit. The digital ramp in the ADC should have a uniform step size of 15mV. Day to day variationsin the performance are within accepted limits of system accuracy. Occasional calibrations at the end of a month is desirable. The following steps should be performed in sequence.

i) Check the low voltage supply to 3.6±.1V.

ii) Check and adjust the reference output to 960 mV with a Digital voltmeter.

iii) Remove the cards C3.3 and C3.4 from the bin A and instead of 1 MHz. clock connect a monopulse generator to pin D of C3.3. This circuit gives out one narrow pulse when a button is pressed.

iv) Clear the flipflops and set Q_7 only. Output at L should be now 960 mV. If not, adjust R_7 to get 960 mV at L.

v) Clear ADC and set Q_6 only. Output at L should now be 480 mV. If not adjusted the R_6 to get 480 mV at L.

vi) Continue the process till Q_1.

vii) Repeat the steps iv - vi till a binary decrement is strictly observed from step (iv) onward.

viii) Connect C to ground and monitor the output at L. It should be within $\pm$ 3mV and stay within this limit for long time runs of the order of an hour. If it changes the 'offset' adjustment on C3.4 should be very carefully adjusted to annull it.

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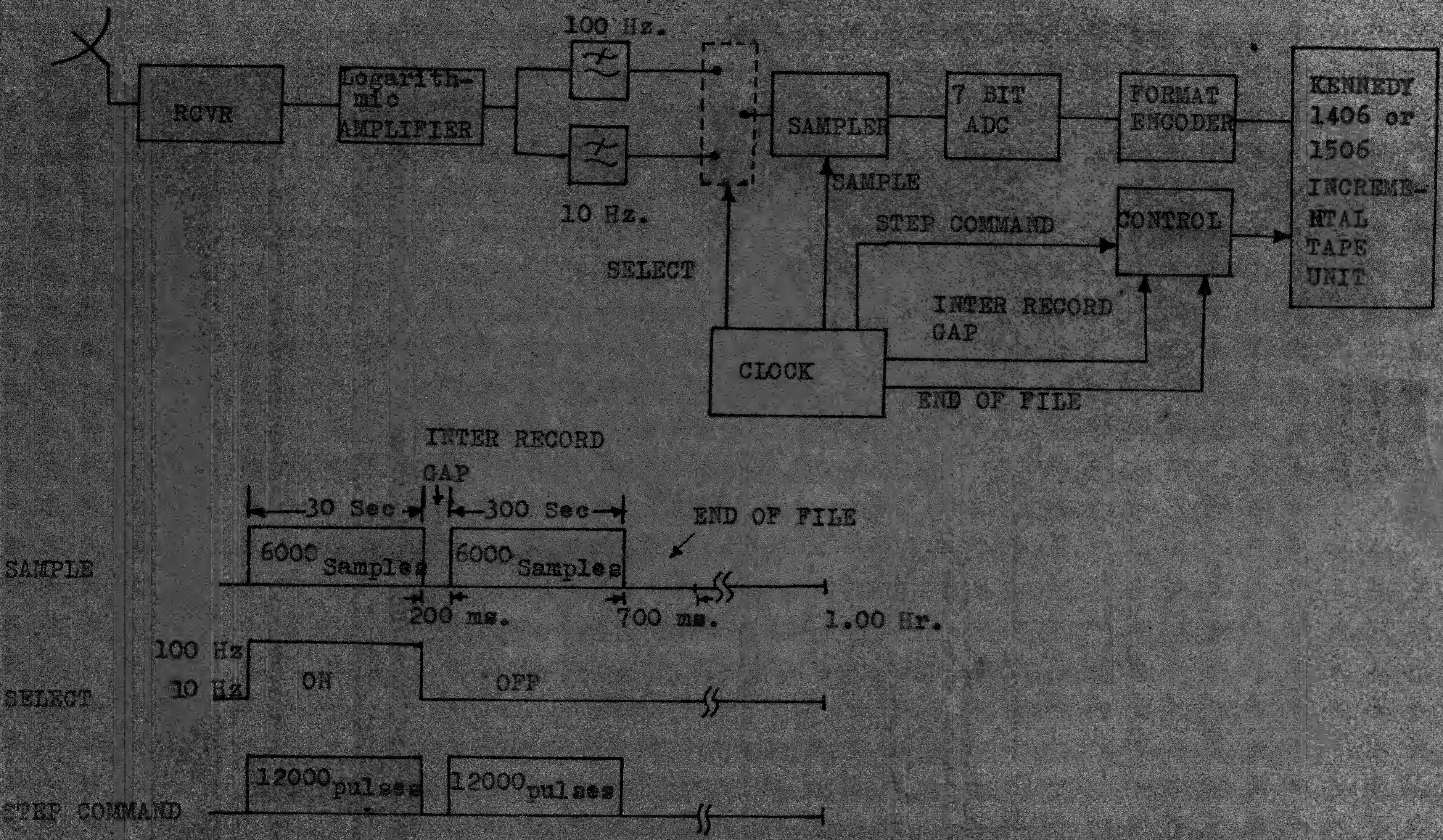


FIGURE 1.1 : A DATA LOGGING SYSTEM USING AN INCREMENTAL DIGITAL TAPE UNIT

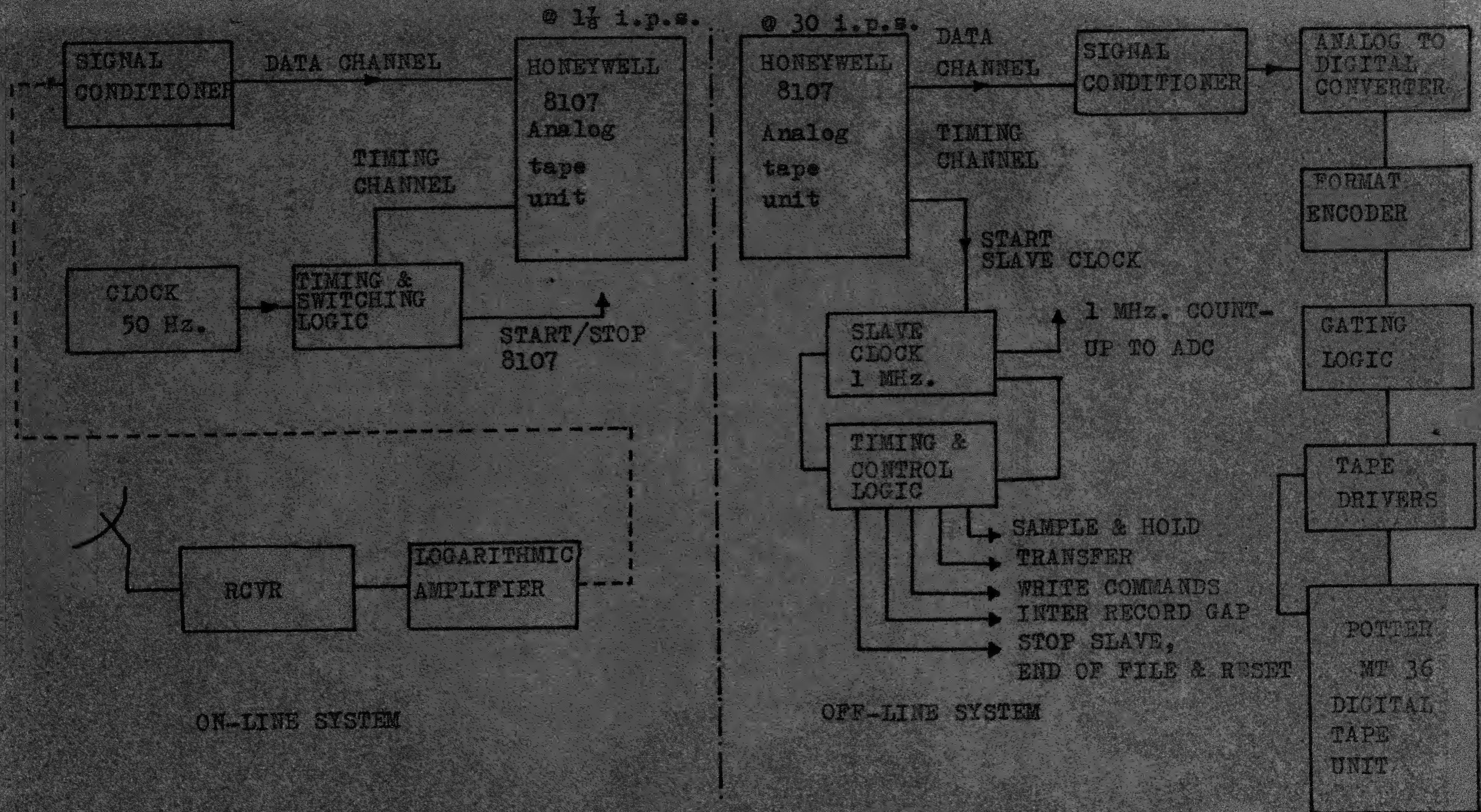


FIGURE 1.2 : THE DIGITAL DATA LOGGING SYSTEM

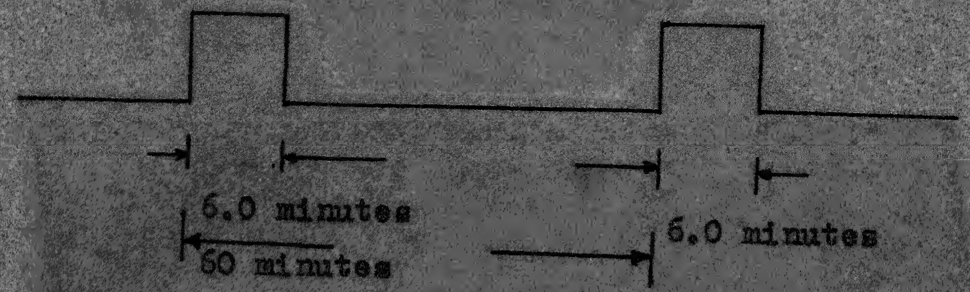


FIGURE 2.1 : TIMING SIGNAL

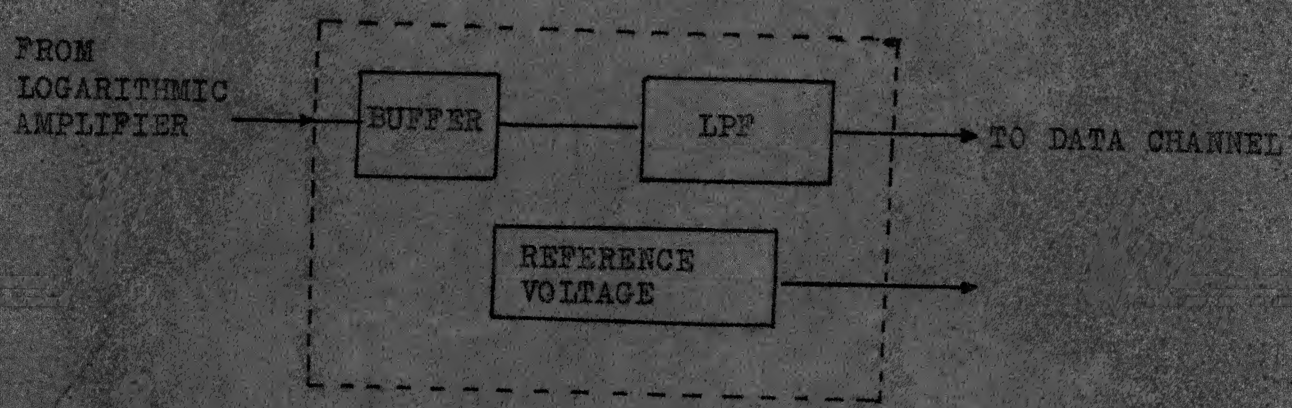


FIGURE 2.2 : SIGNAL CONDITIONING

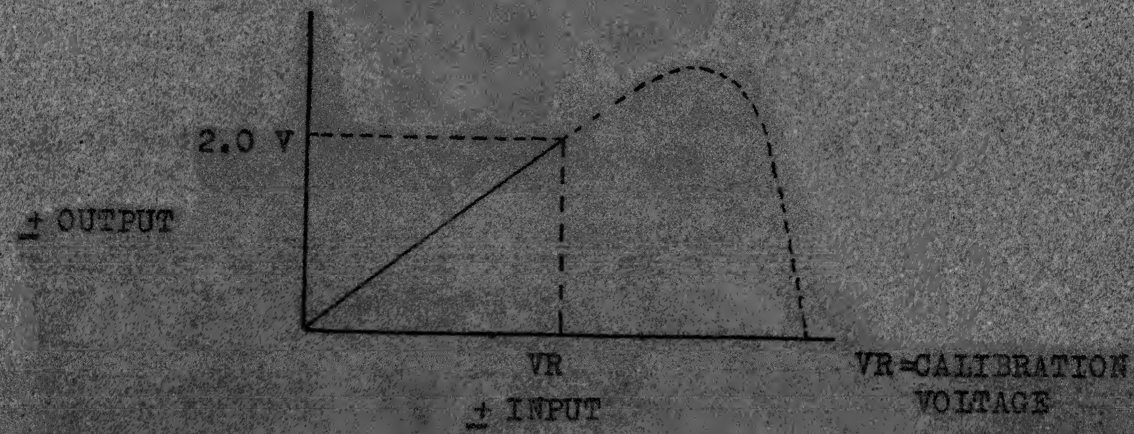


FIGURE 2.3 : TRANSFER CHARACTERISTIC OF THE ANALOG TAPE RECORDER

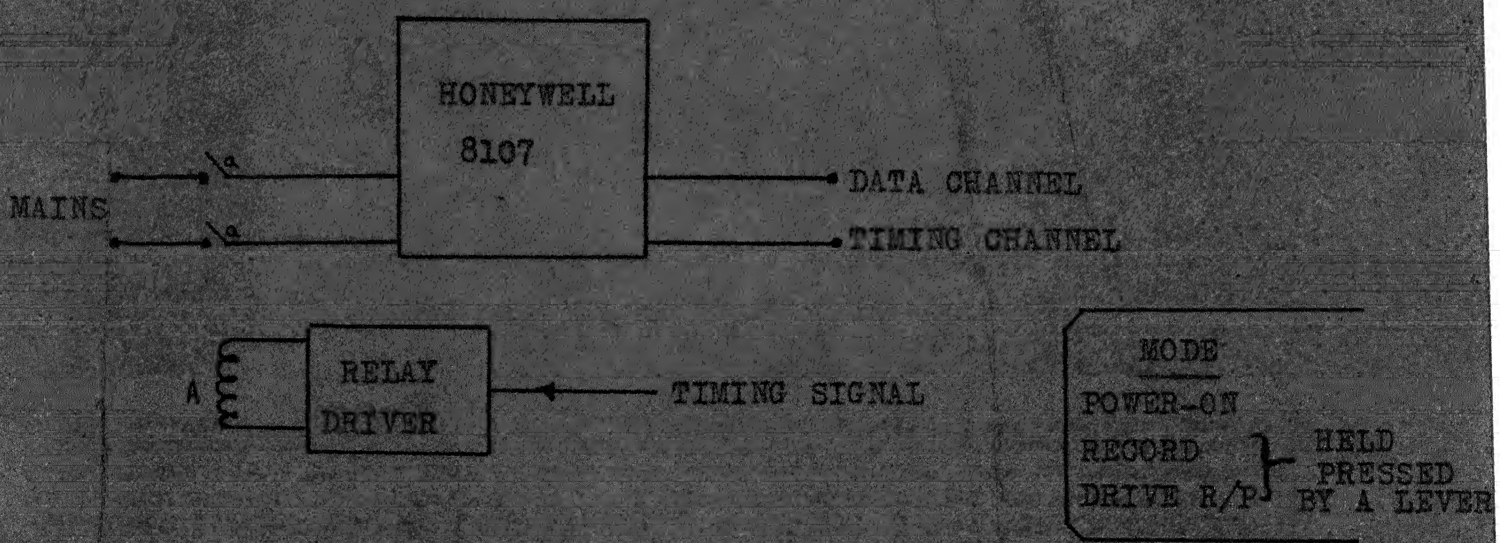
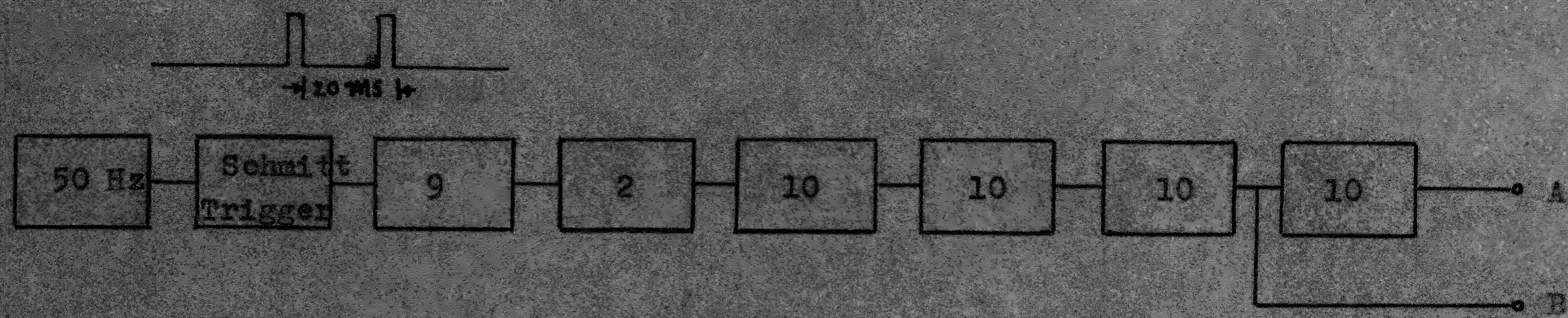
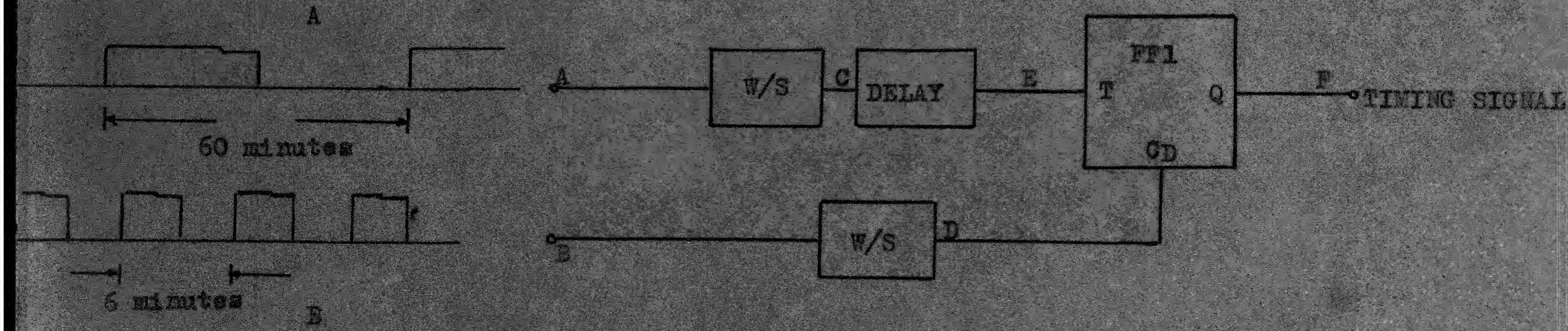


FIGURE 2.4 : ON-LINE ANALOG RECORDING



(a)



(b)

FIGURE 2.5: GENERATION OF TIMING SIGNAL

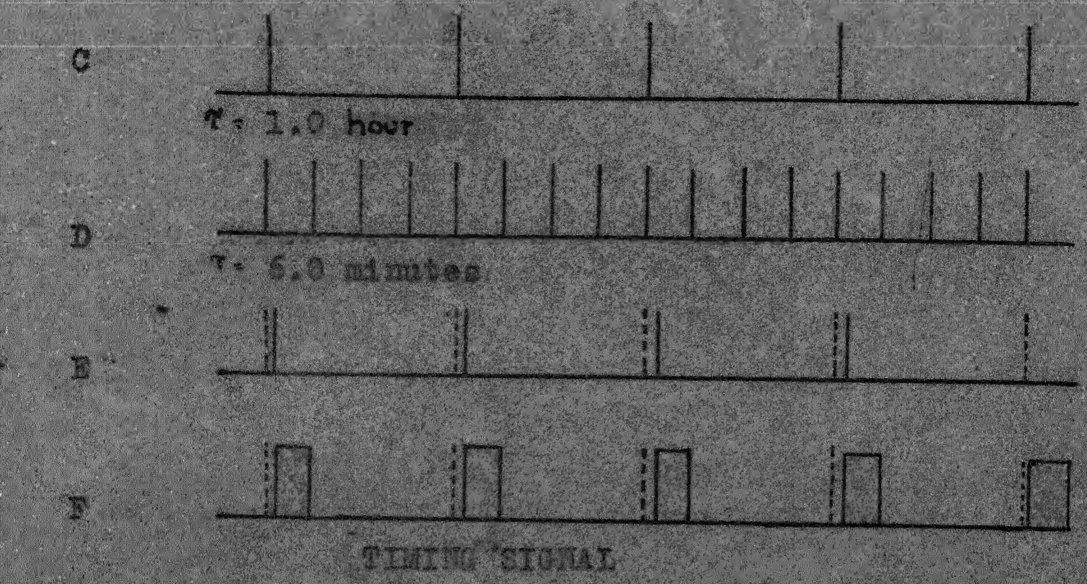


FIGURE 2.6 : TIMING DIAGRAM

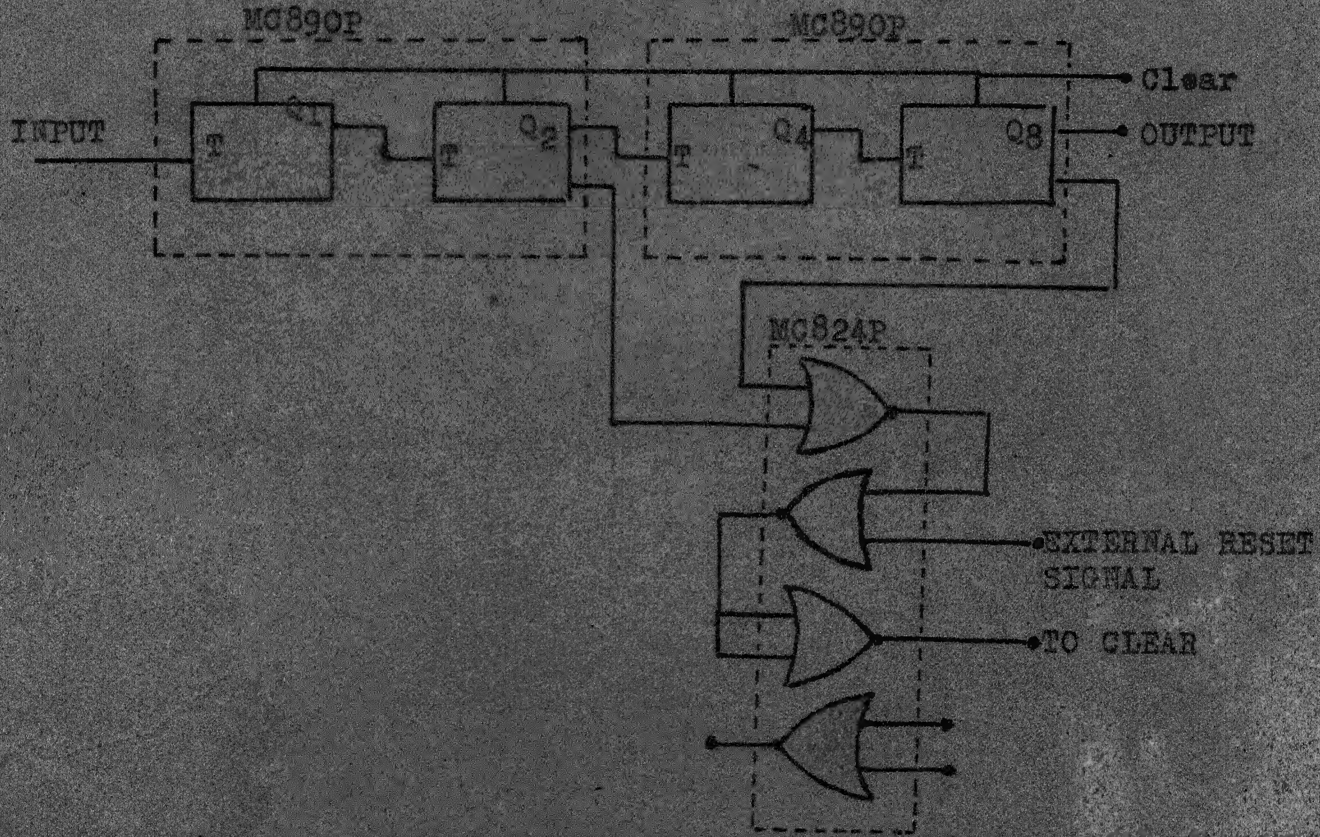


FIGURE 2.7 : DECADE COUNTER CARD

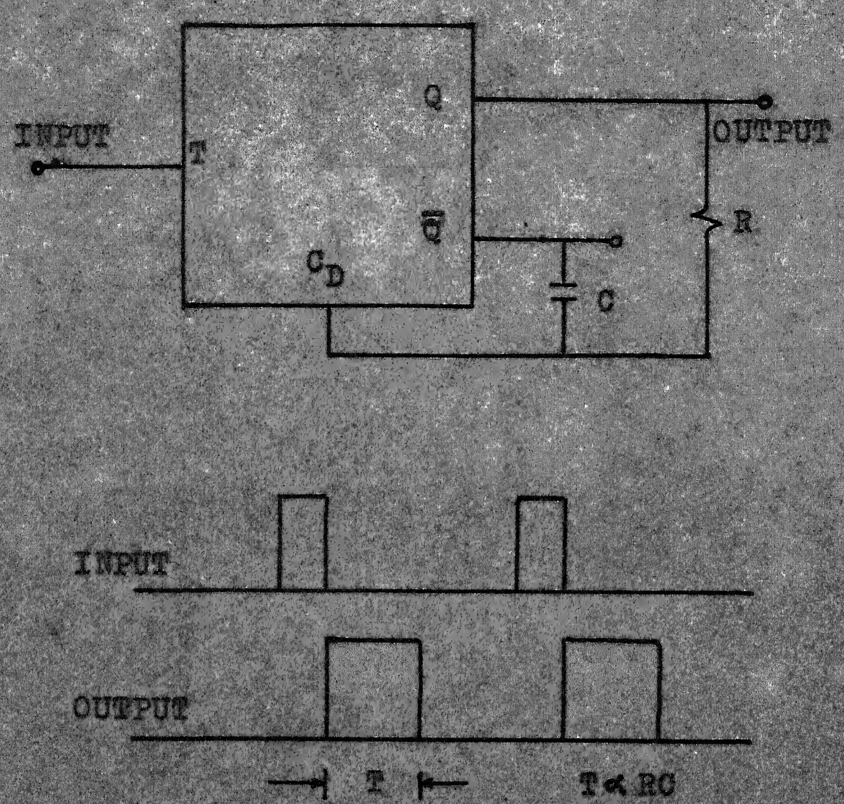


FIGURE 2.8 : DELAY GENERATION

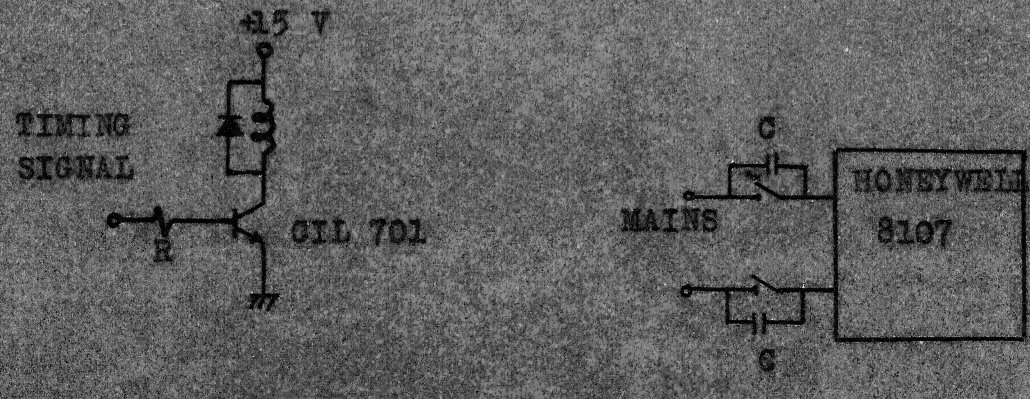
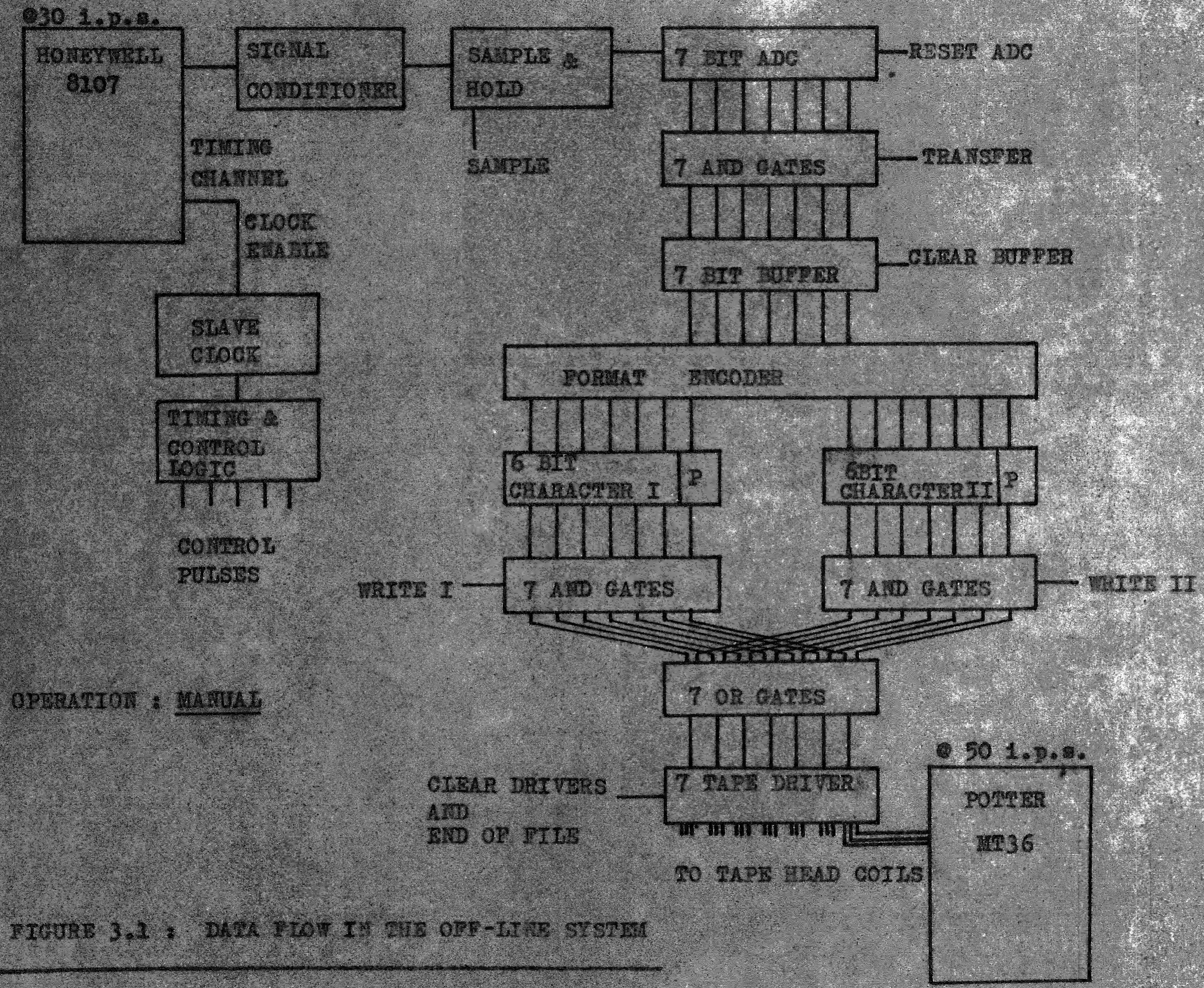
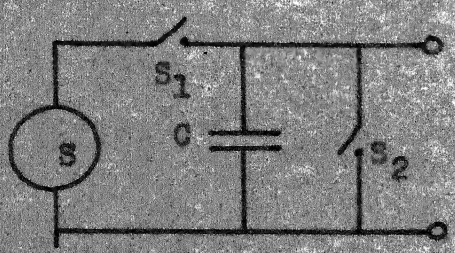


FIGURE 2.9 : RELAY DRIVER



OPERATION : MANUAL

FIGURE 3.1 : DATA FLOW IN THE OFF-LINE SYSTEM



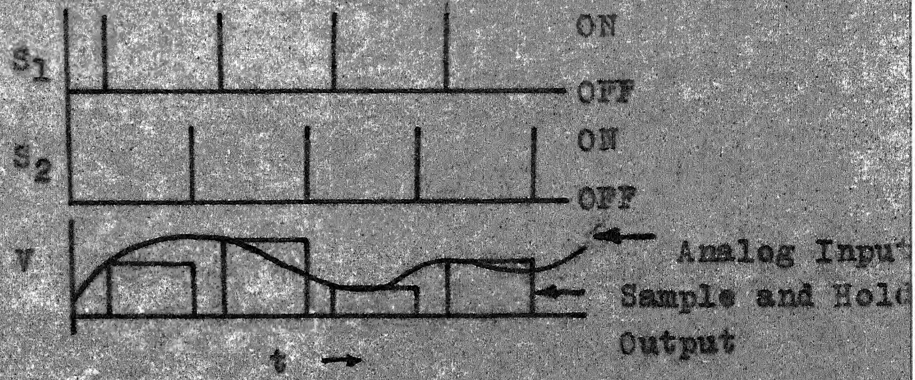


FIGURE 3.2 a : BASIC SAMPLE AND HOLD CIRCUIT

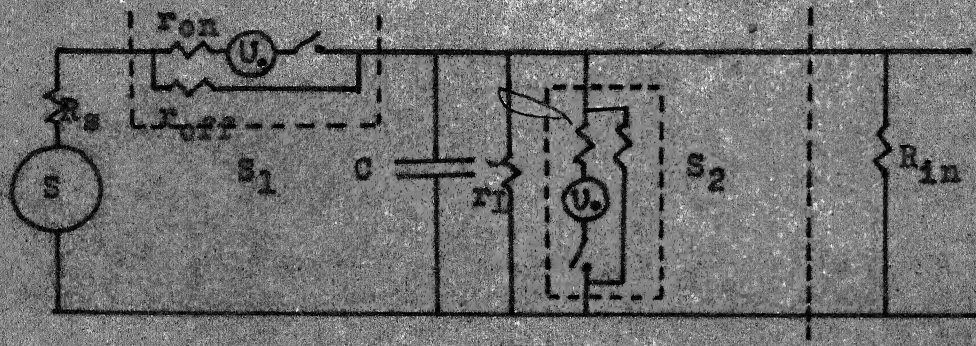


FIGURE 3.2 b : SOURCES OF ERROR IN SAMPLE AND HOLD CIRCUIT

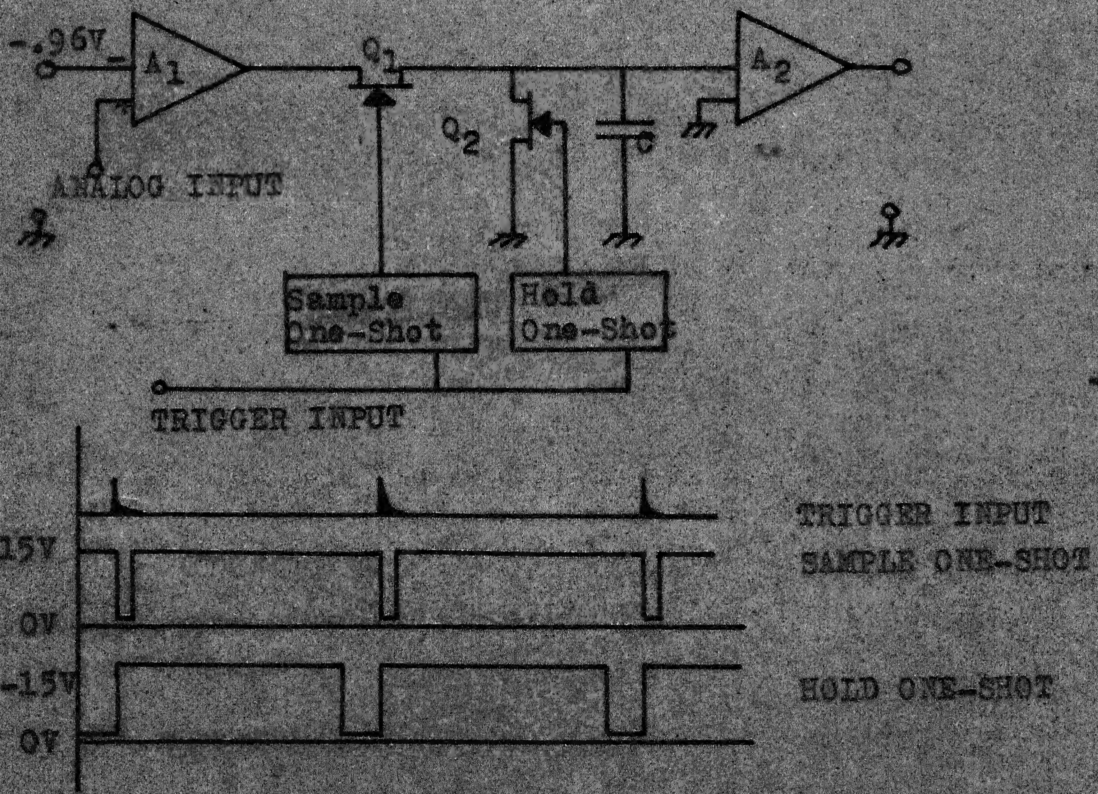


FIGURE 3.2 c : SCHEMATIC OF SAMPLE AND HOLD CIRCUIT

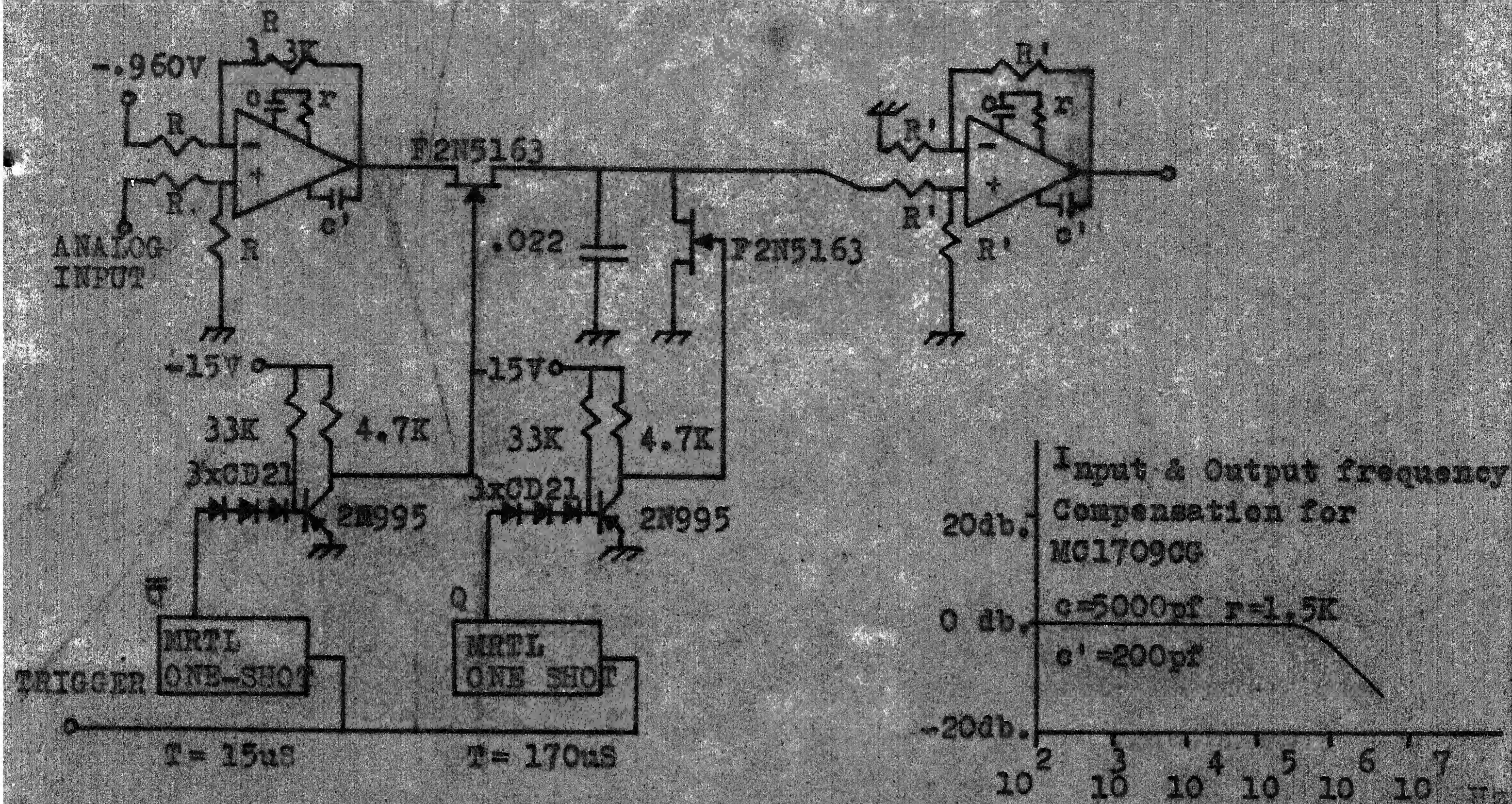


FIGURE 3.2 d : CIRCUIT DIAGRAM OF THE SAMPLE AND HOLD

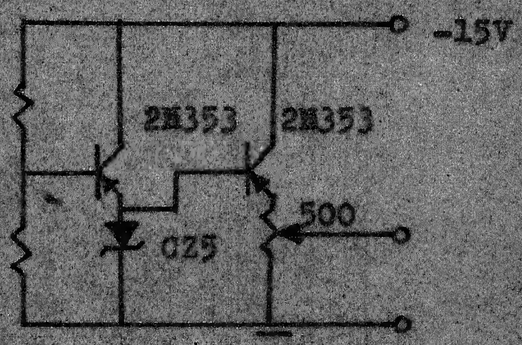


FIGURE 3.2 e : REFERENCE VOLTAGE SOURCE

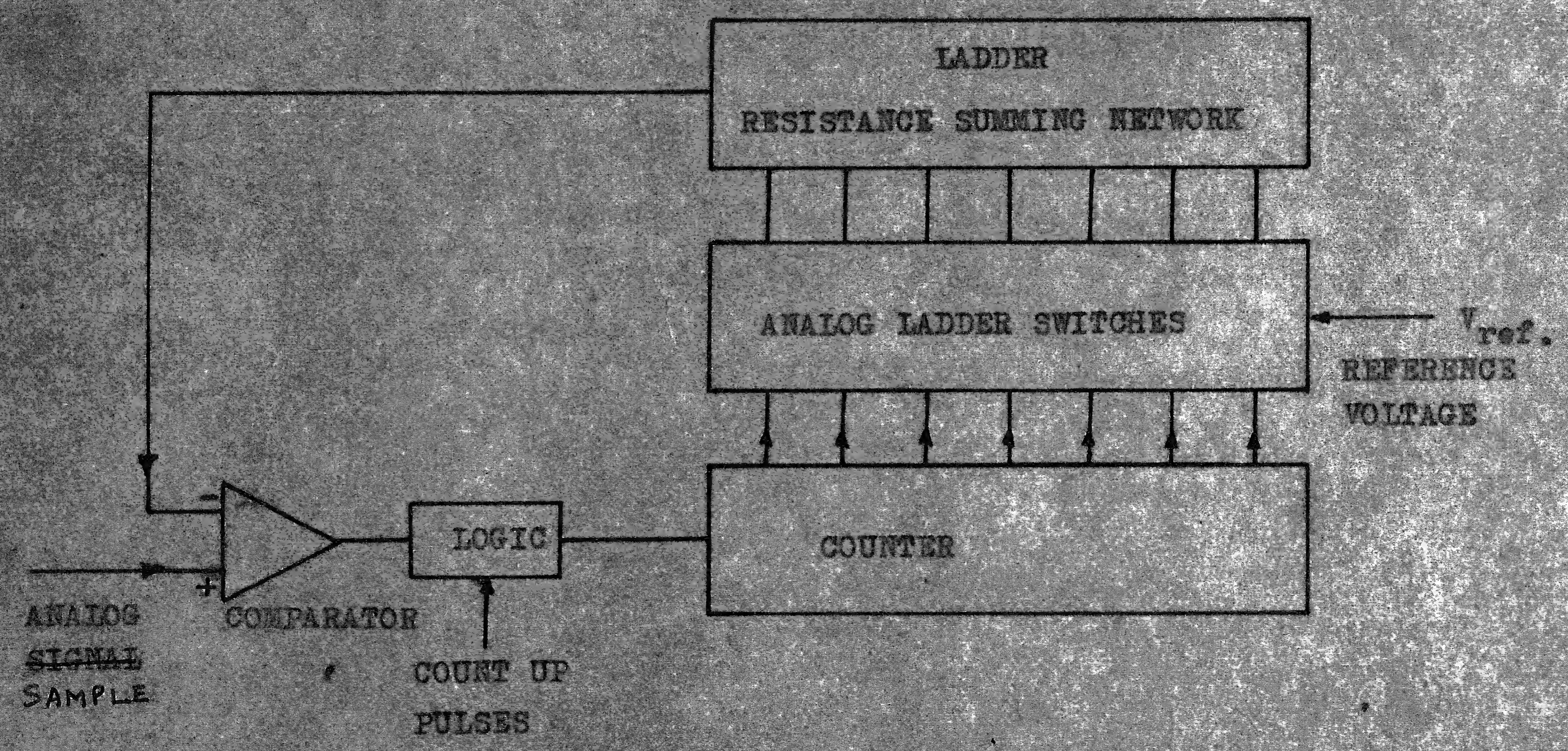


FIGURE 3.3 a : BASIC ANALOG TO DIGITAL CONVERTER

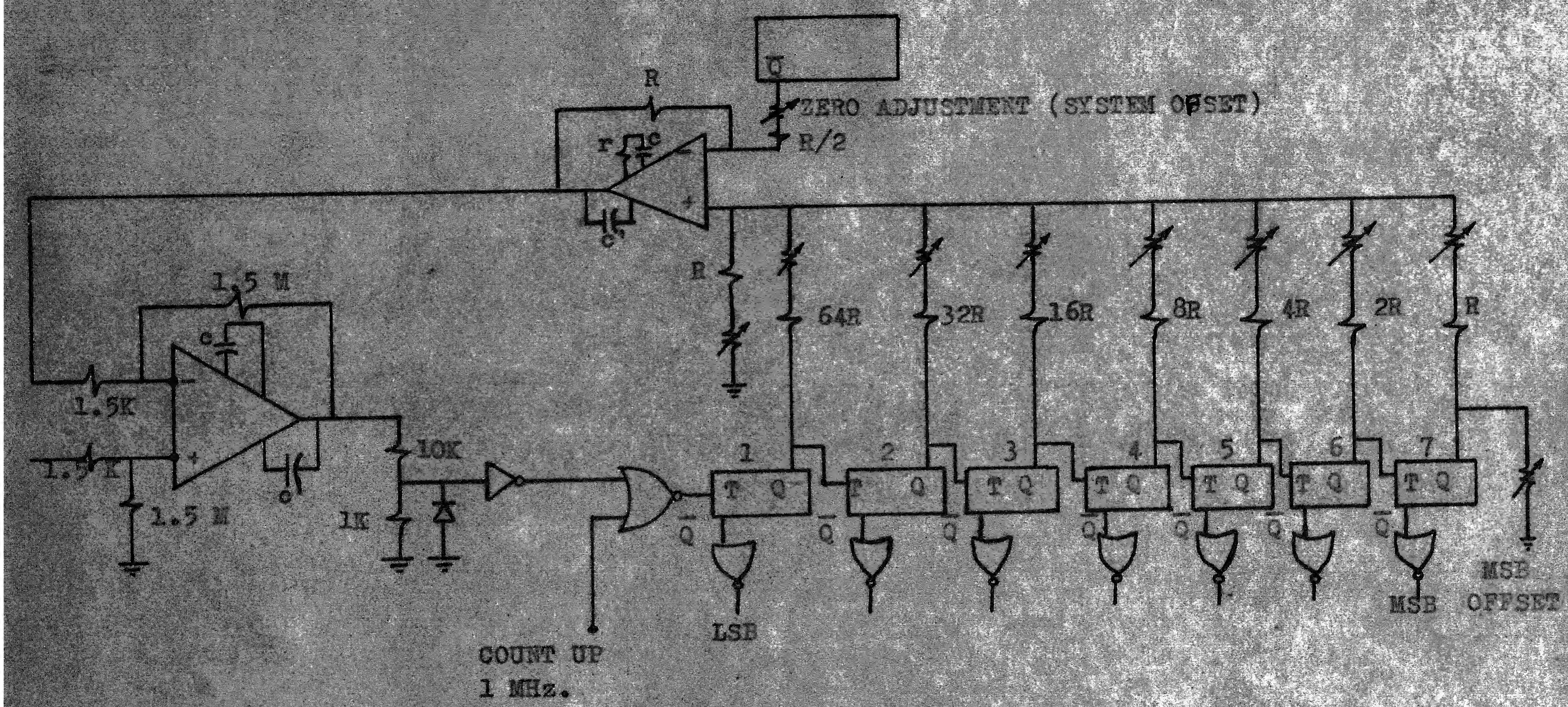


FIGURE 3.3 b : ANALOG TO DIGITAL CONVERTER

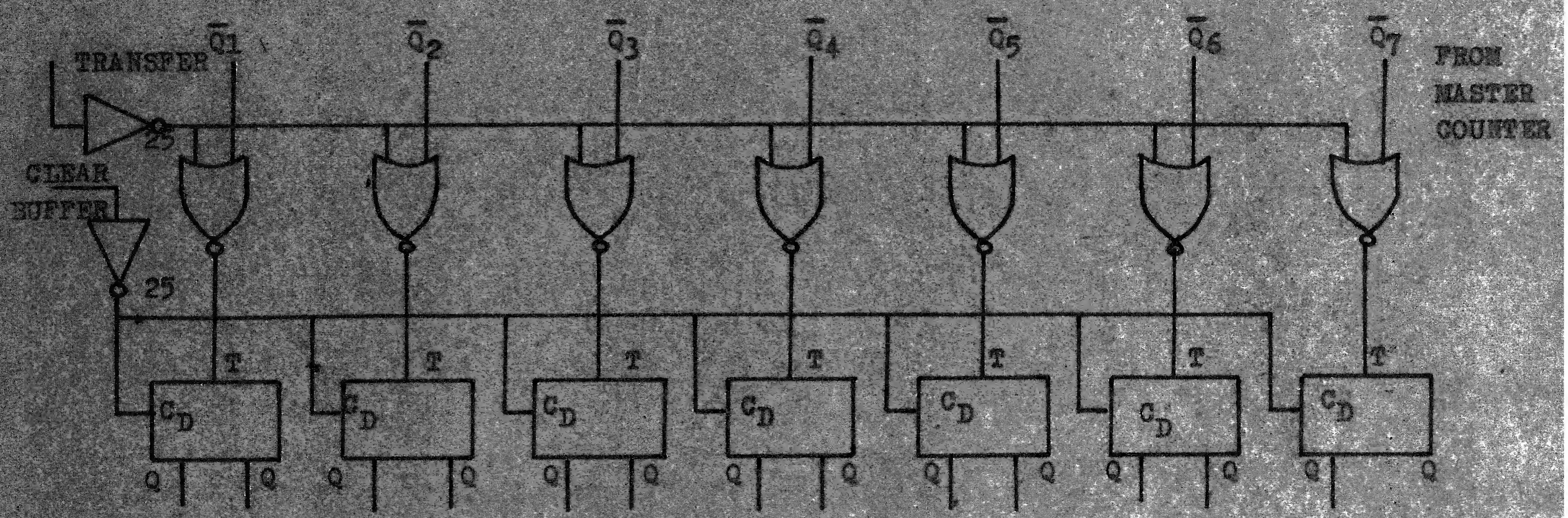


FIGURE 3.4 : TRANSFER TO BUFFER CIRCUIT

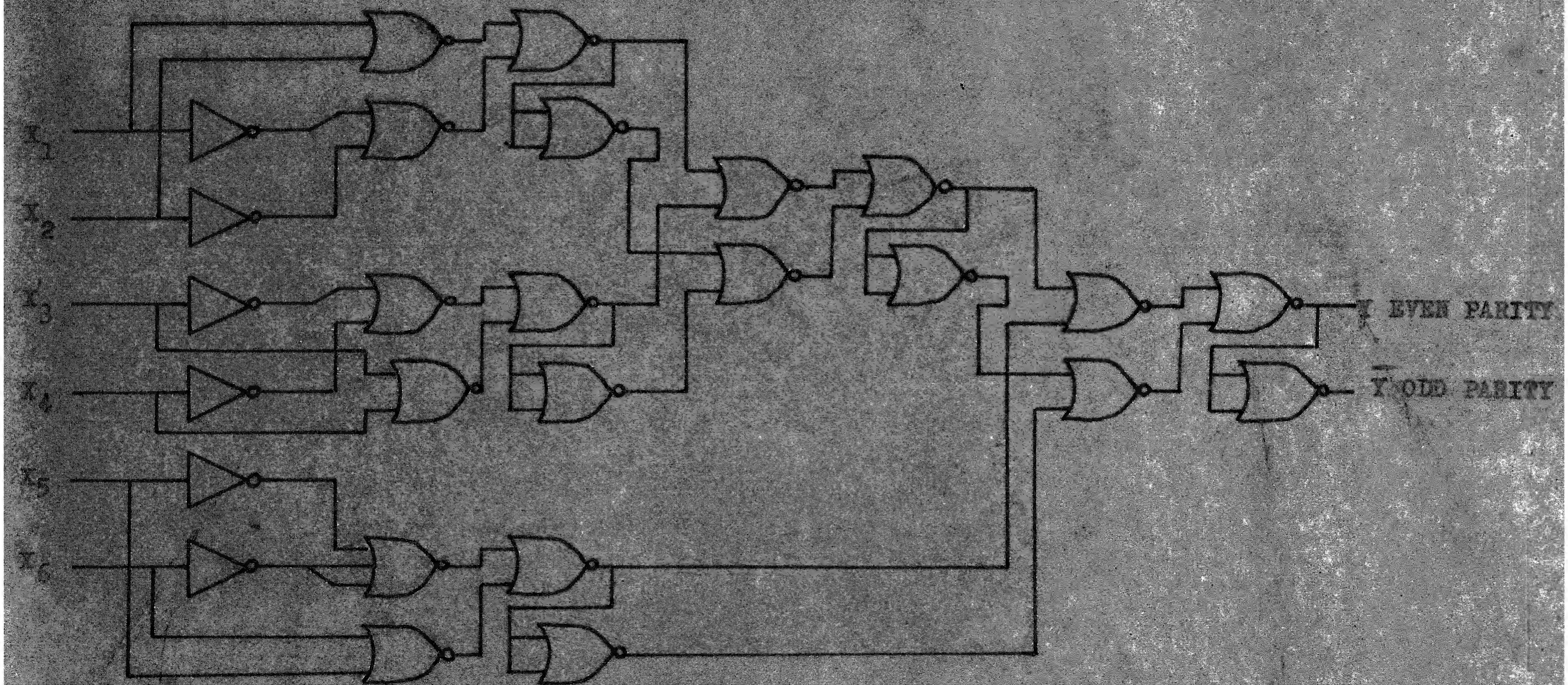


FIGURE 3.6 : CHARACTER PARITY GENERATOR

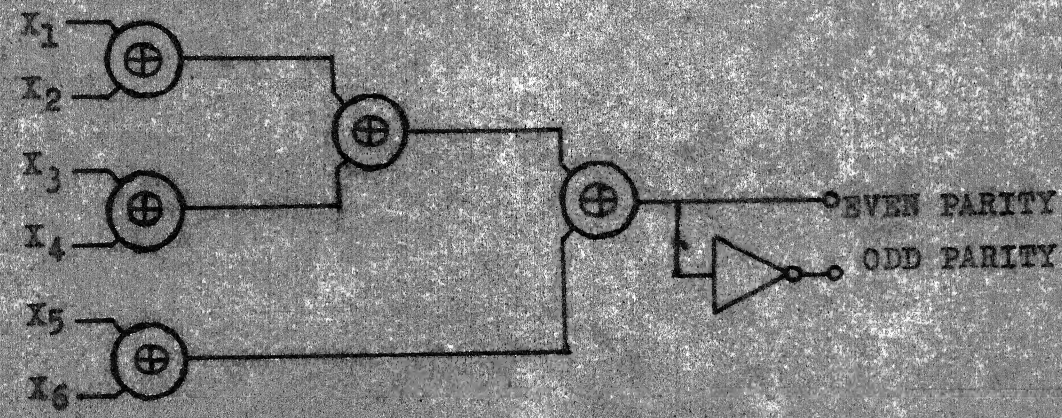


FIGURE 3.6 a : BASIC PARITY CHECKING STRUCTURE

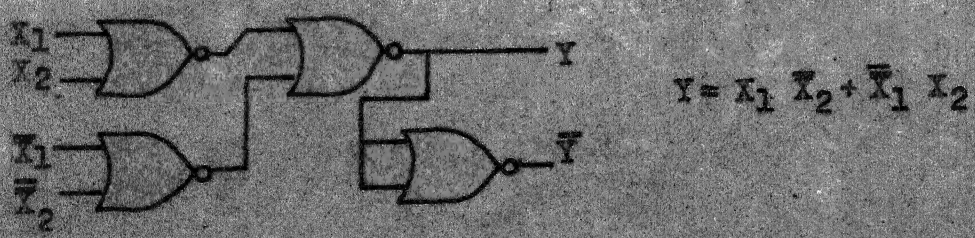


FIGURE 3.6 b : 'EXCLUSIVE OR' IMPLEMENTATION

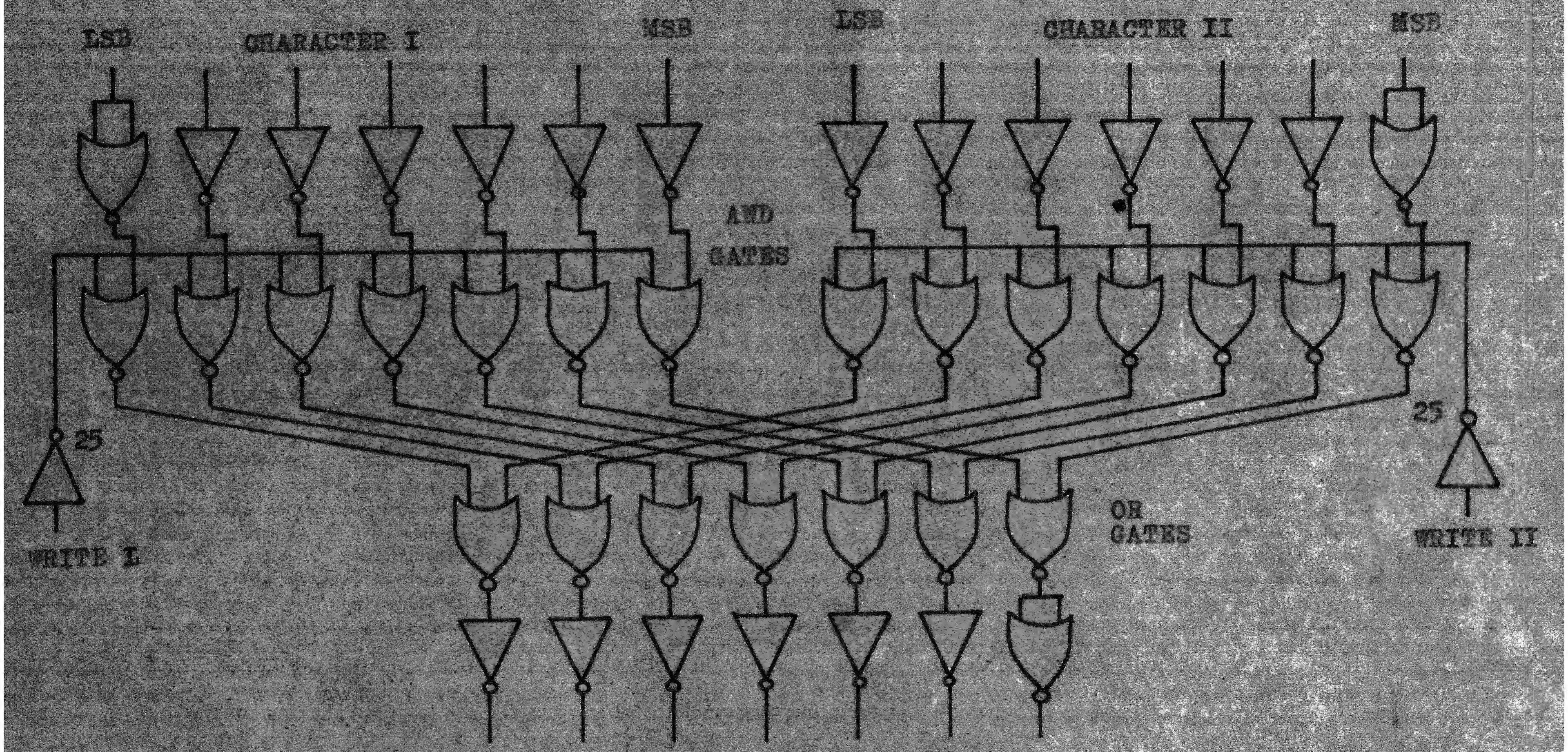


FIGURE 3.7 : WRITING LOGIC

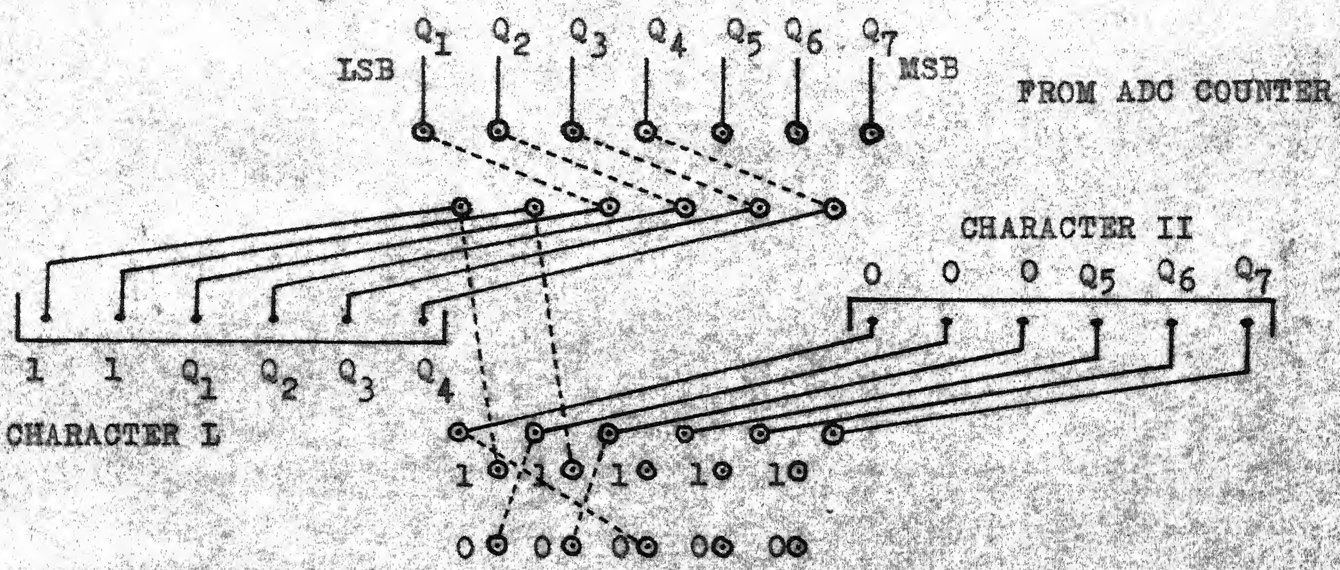


FIGURE 3.5 : PATCH UP CARD

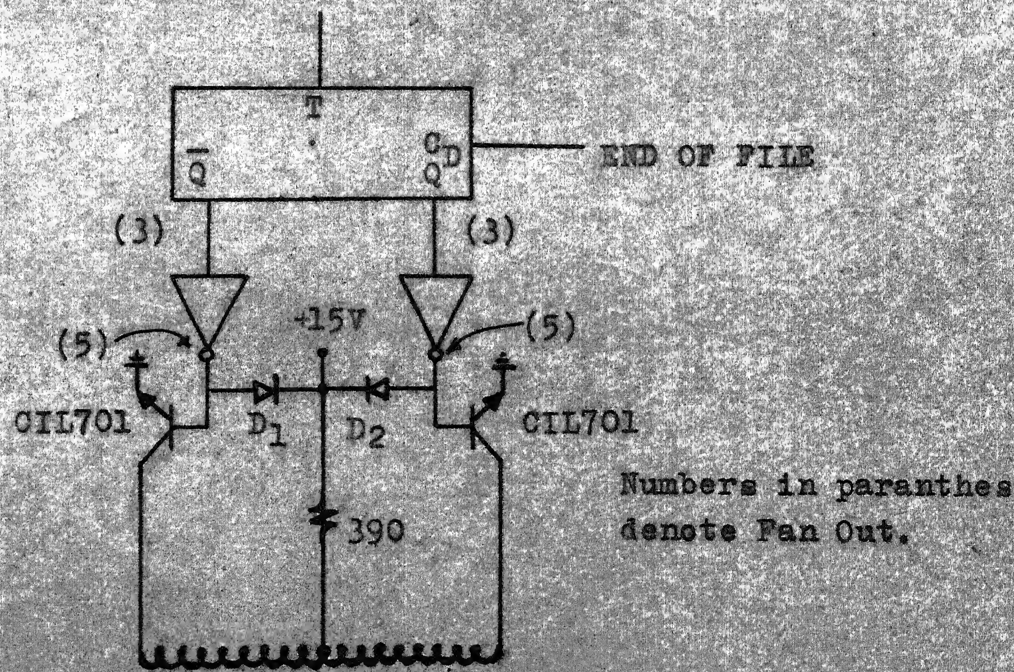


FIGURE 3.8 : TAPE DRIVER CIRCUIT

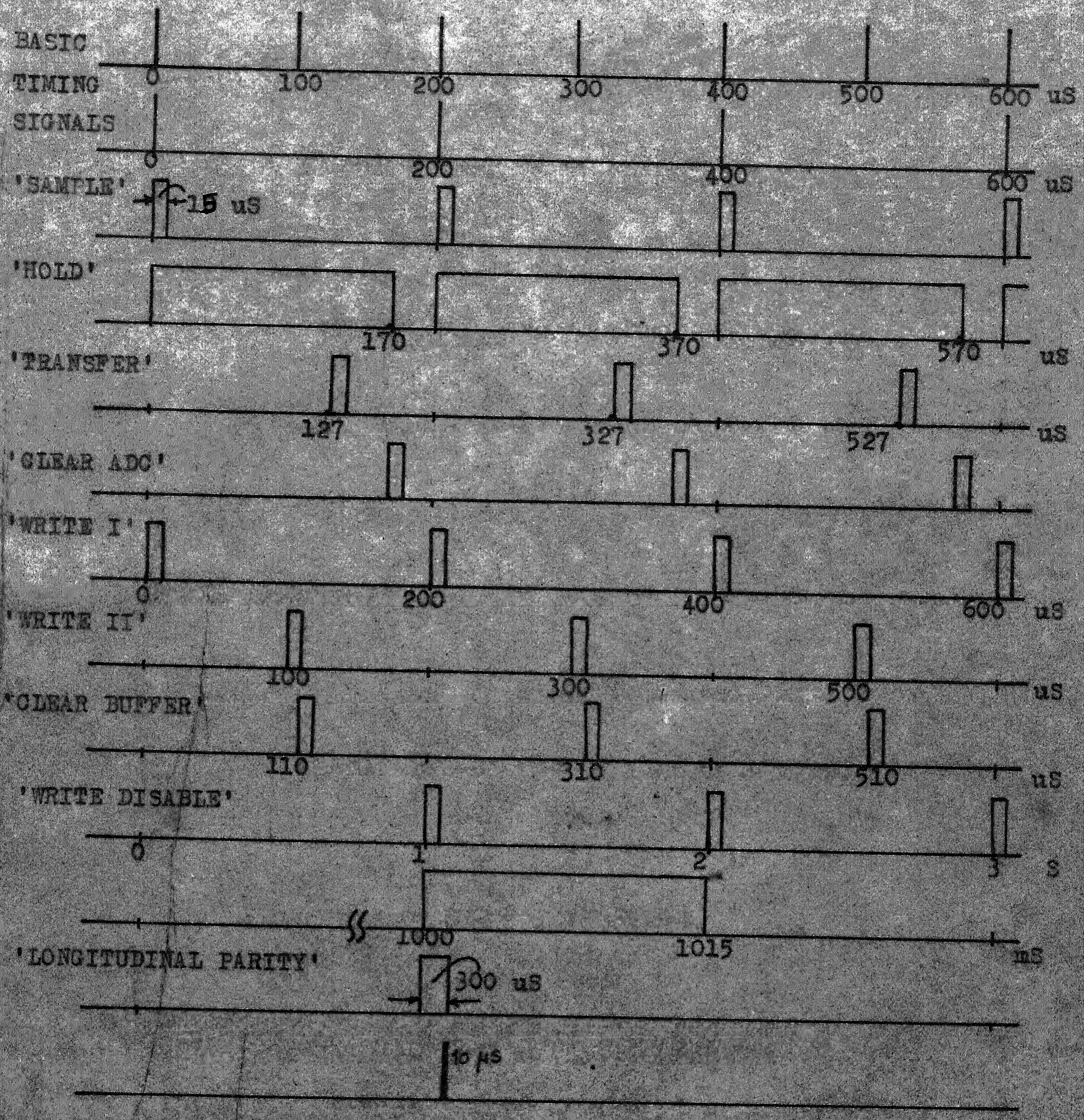


FIGURE 3.9 : TIMING DIAGRAM

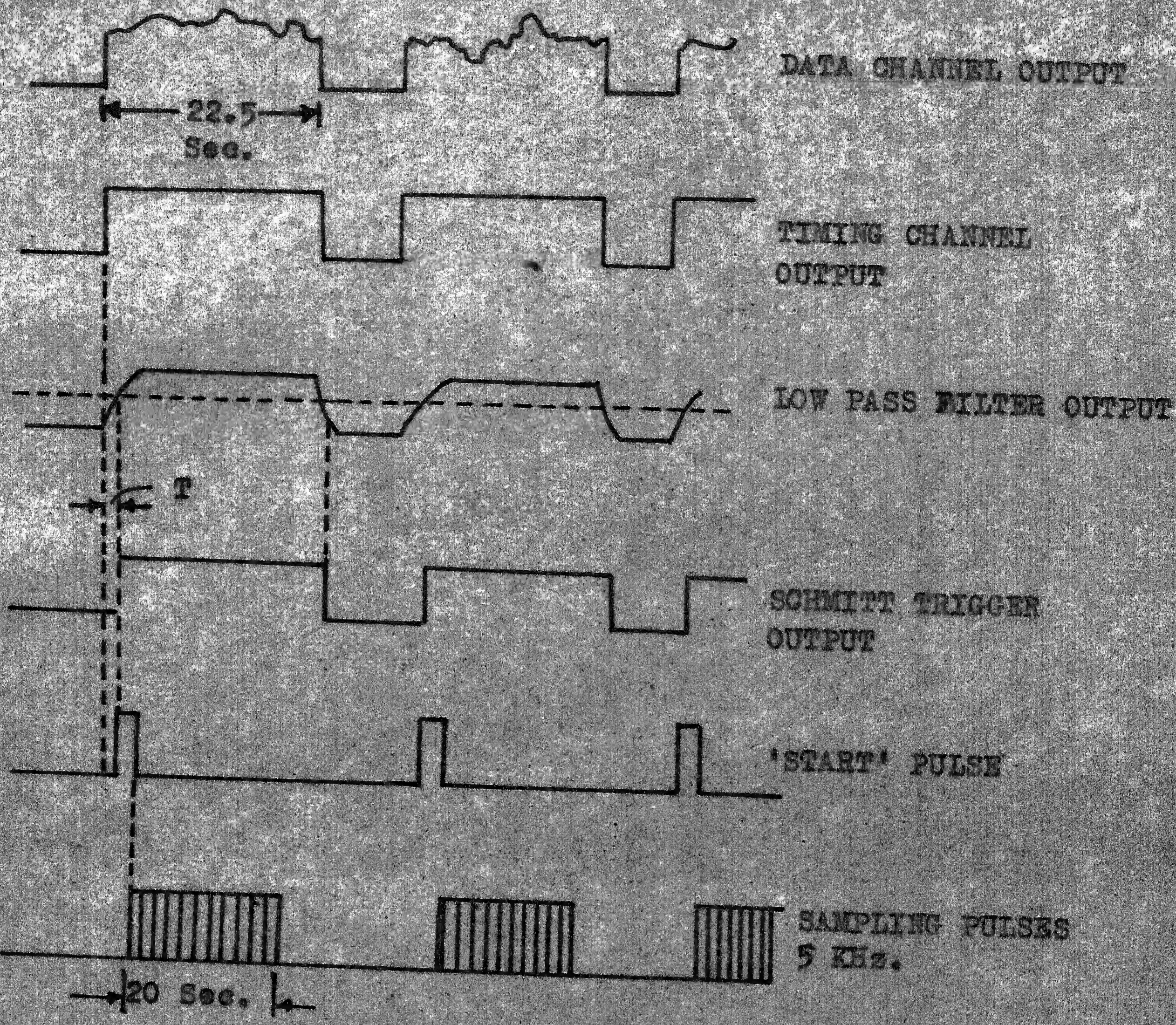


FIGURE 4.1 : TIMING DIAGRAM

FIGURE 4.2 : GENERATION OF 'START' PULSE

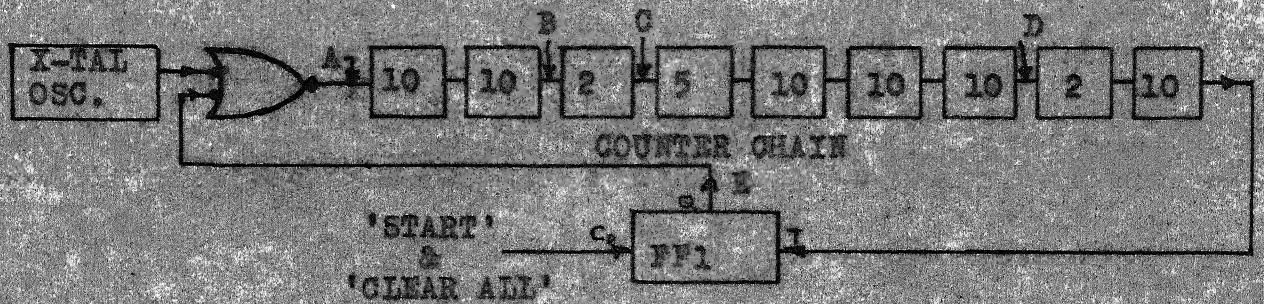


FIGURE 4.3 : BLOCK DIAGRAM OF THE DIGITAL CLOCK

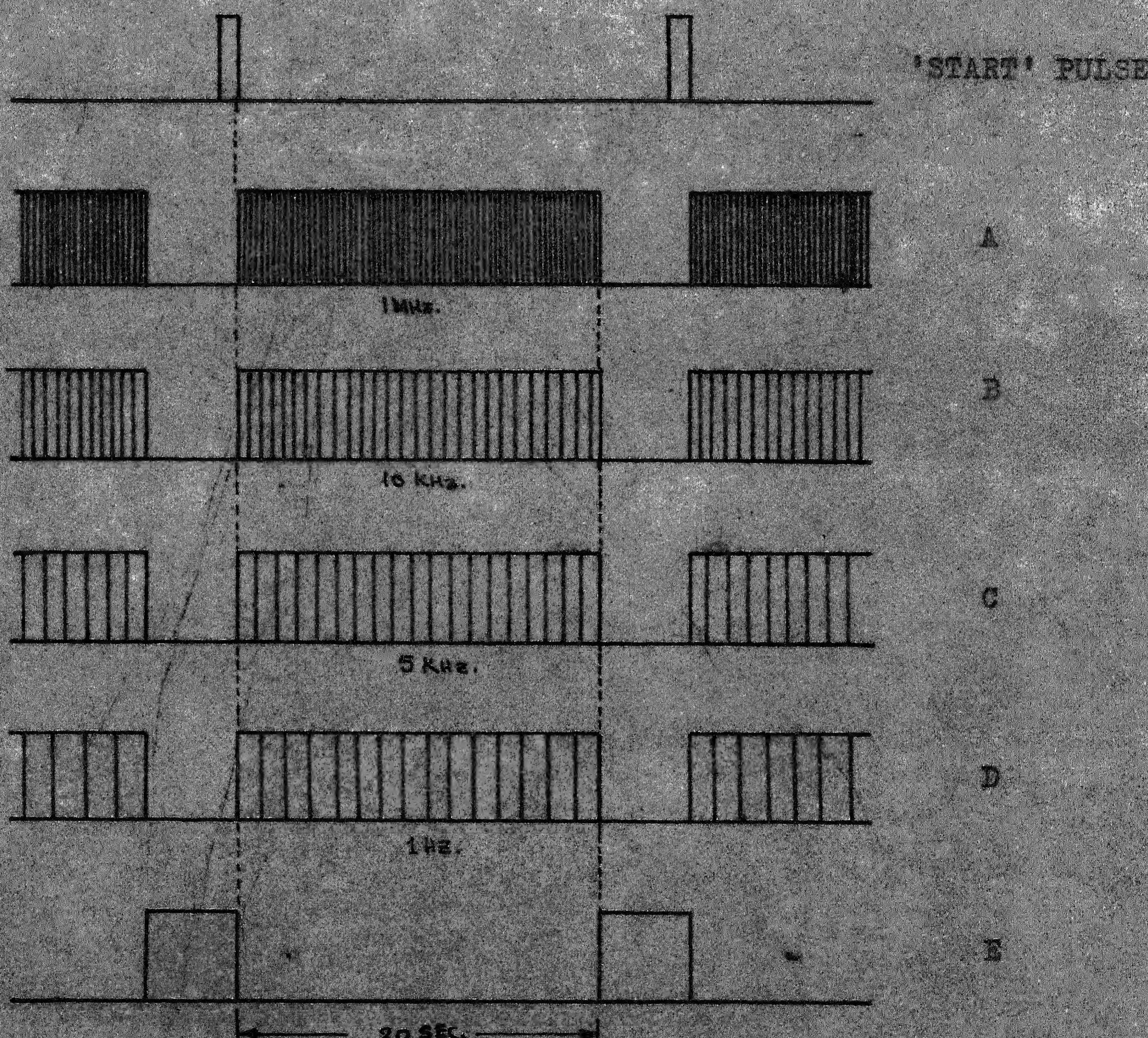


FIGURE 4.4 : TIMING DIAGRAM

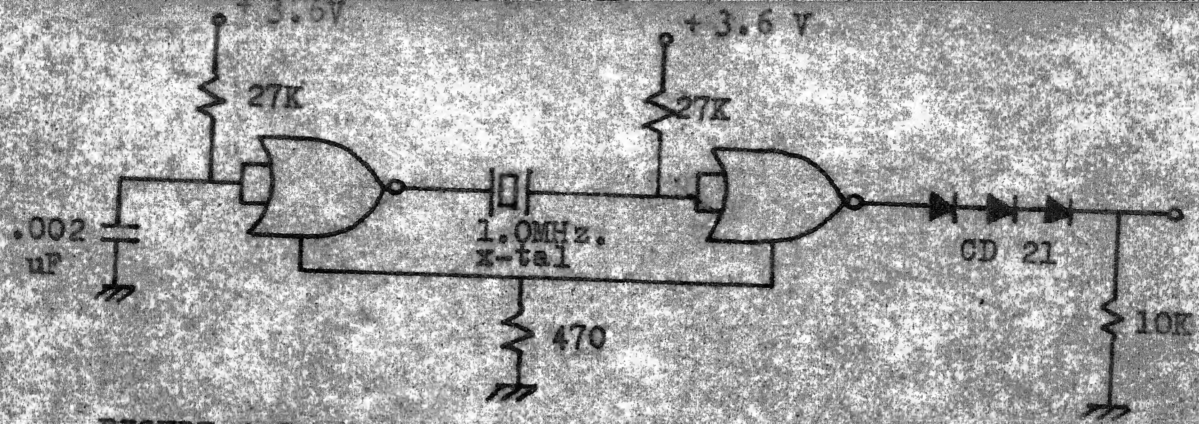


FIGURE 4.5 : CRYSTAL OSCILLATOR

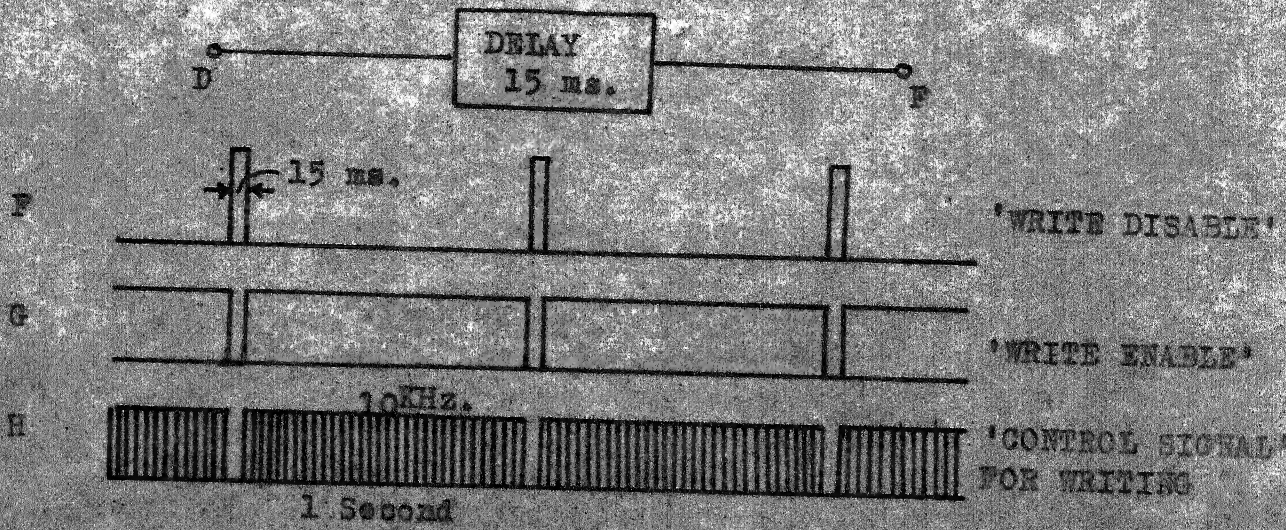


FIGURE 4.6 : INTER RECORD GAP GENERATION

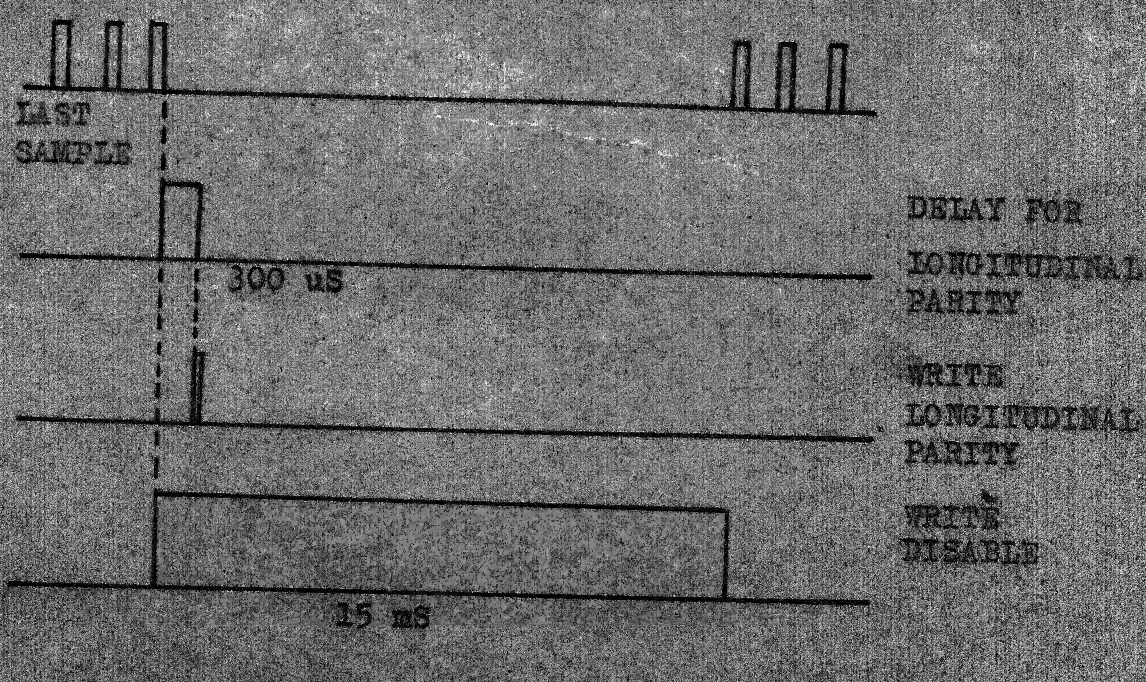


FIGURE 4.7 : TIMING DIAGRAM

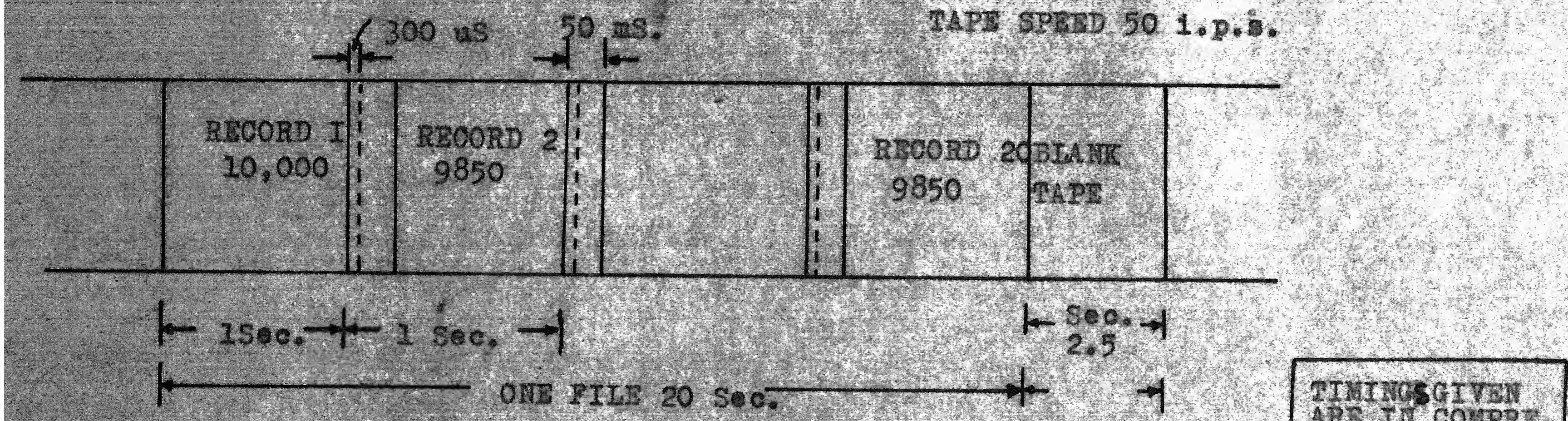


FIGURE 5.1 : FORMAT IN WHICH INFORMATION IS STORED ON DIGITAL TAPE

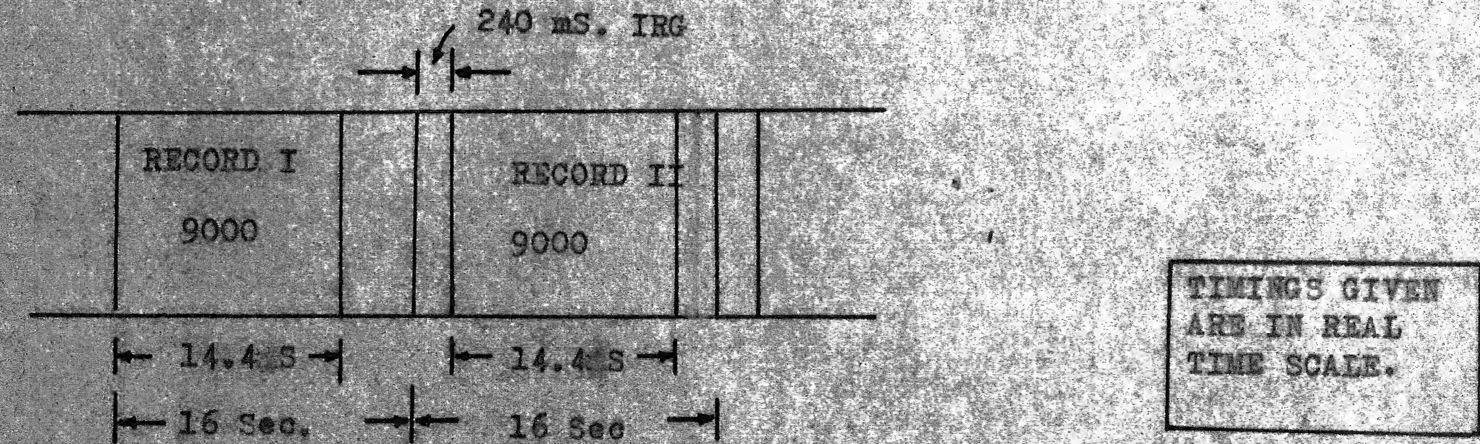


FIGURE 5.2 : PACKING OF FAST FADES

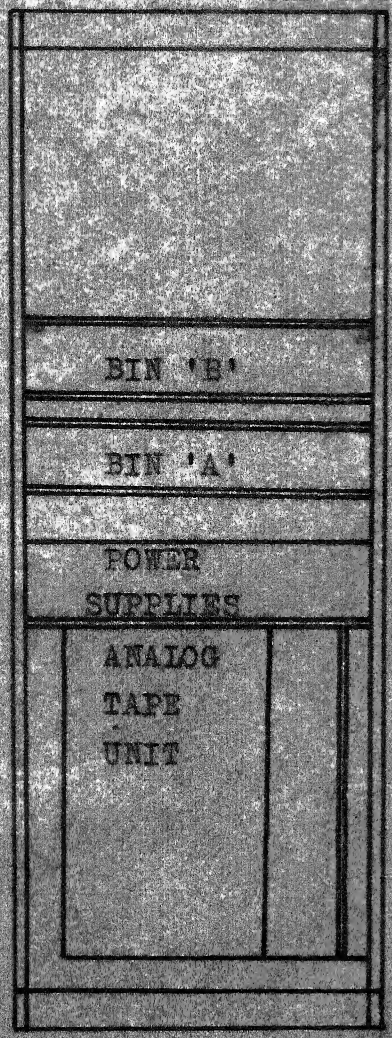


FIGURE 6.1 a : SYSTEM LAY-OUT

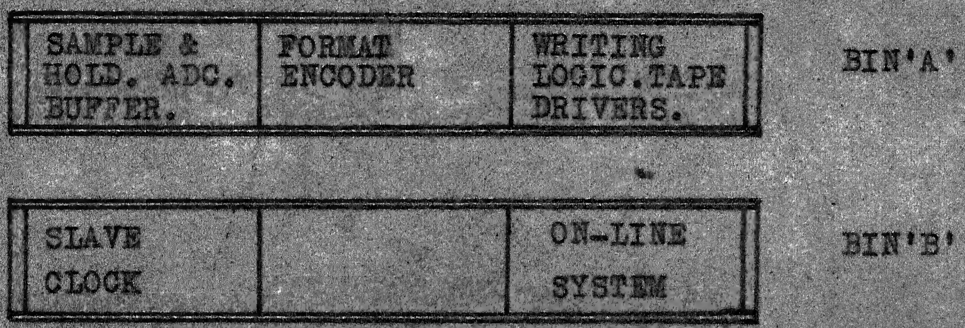


FIGURE 6.1 b: CARD LAY-OUT

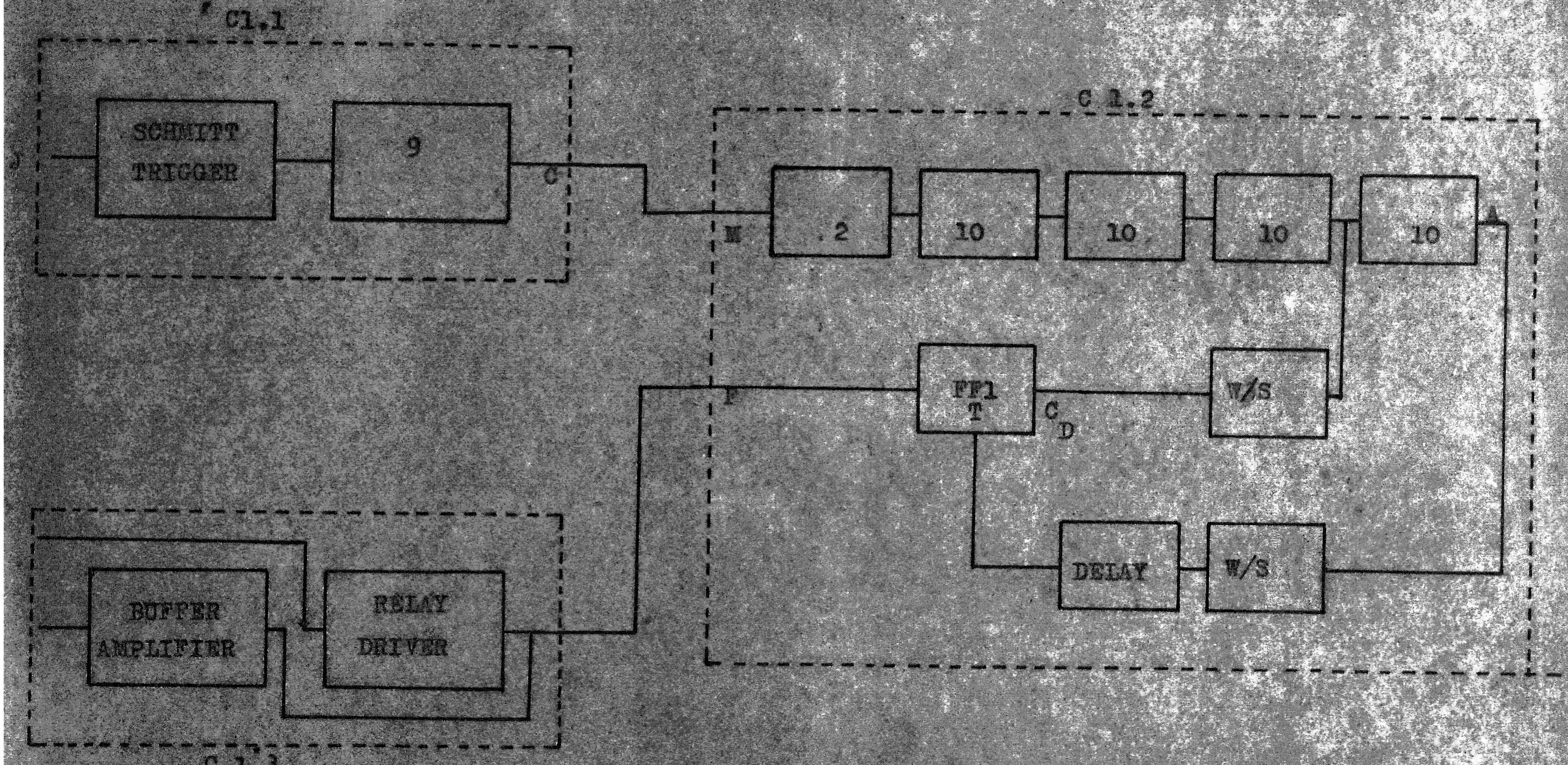


FIGURE 6.2 : LAY-OUT DIAGRAM FOR ON-LINE SYSTEM

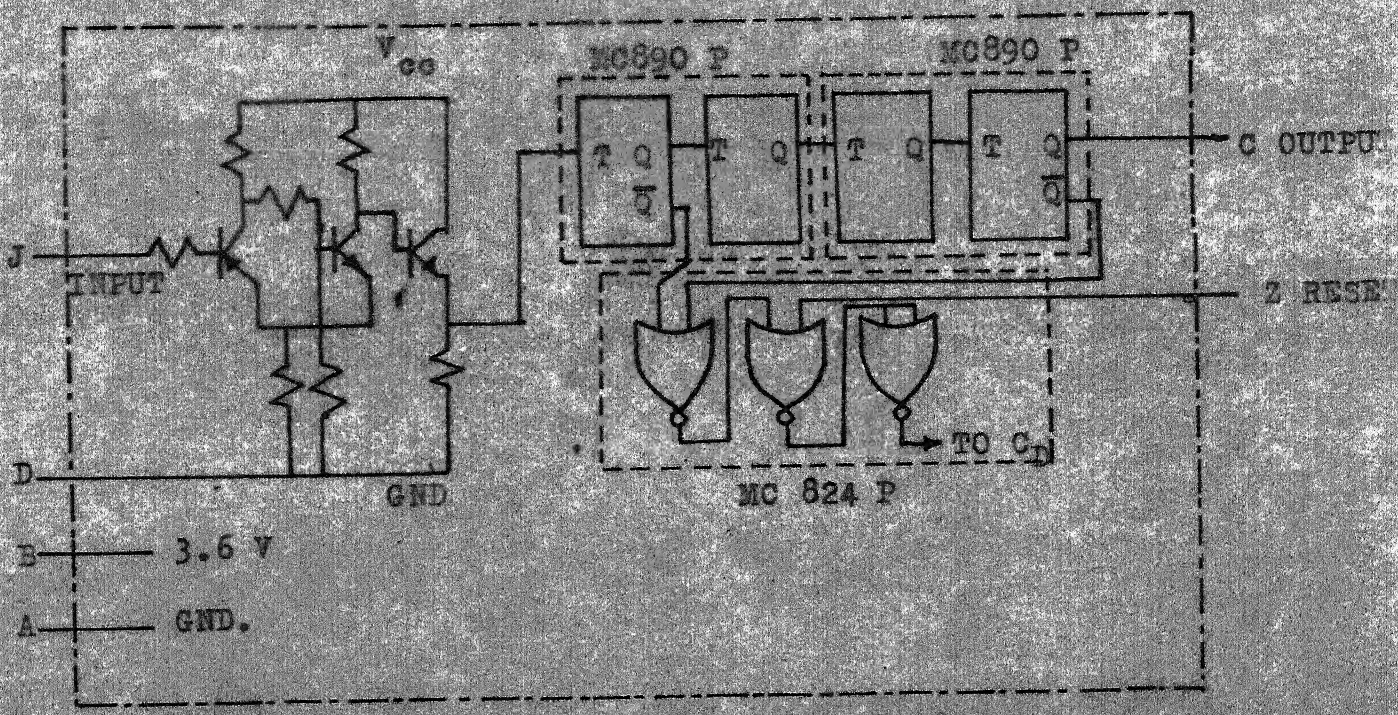


FIGURE 6.3 : DETAILS OF CARD 1.1

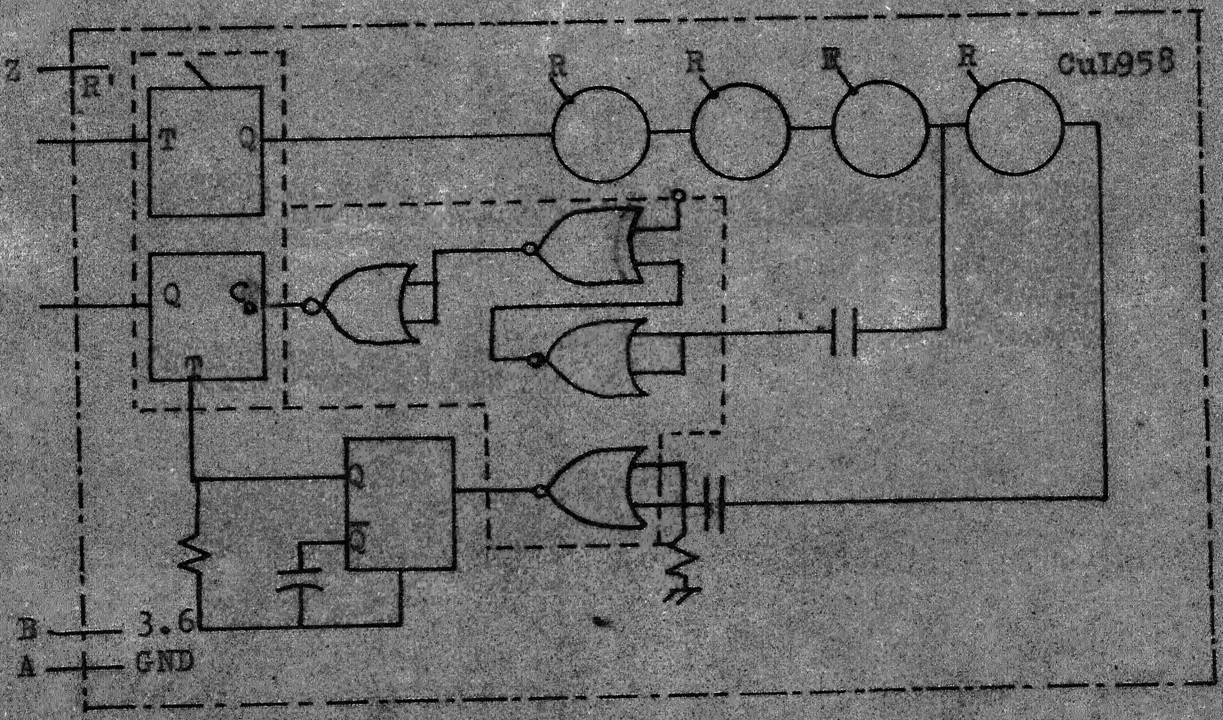


FIGURE 6,4 : DETAILS OF CARD 1.2

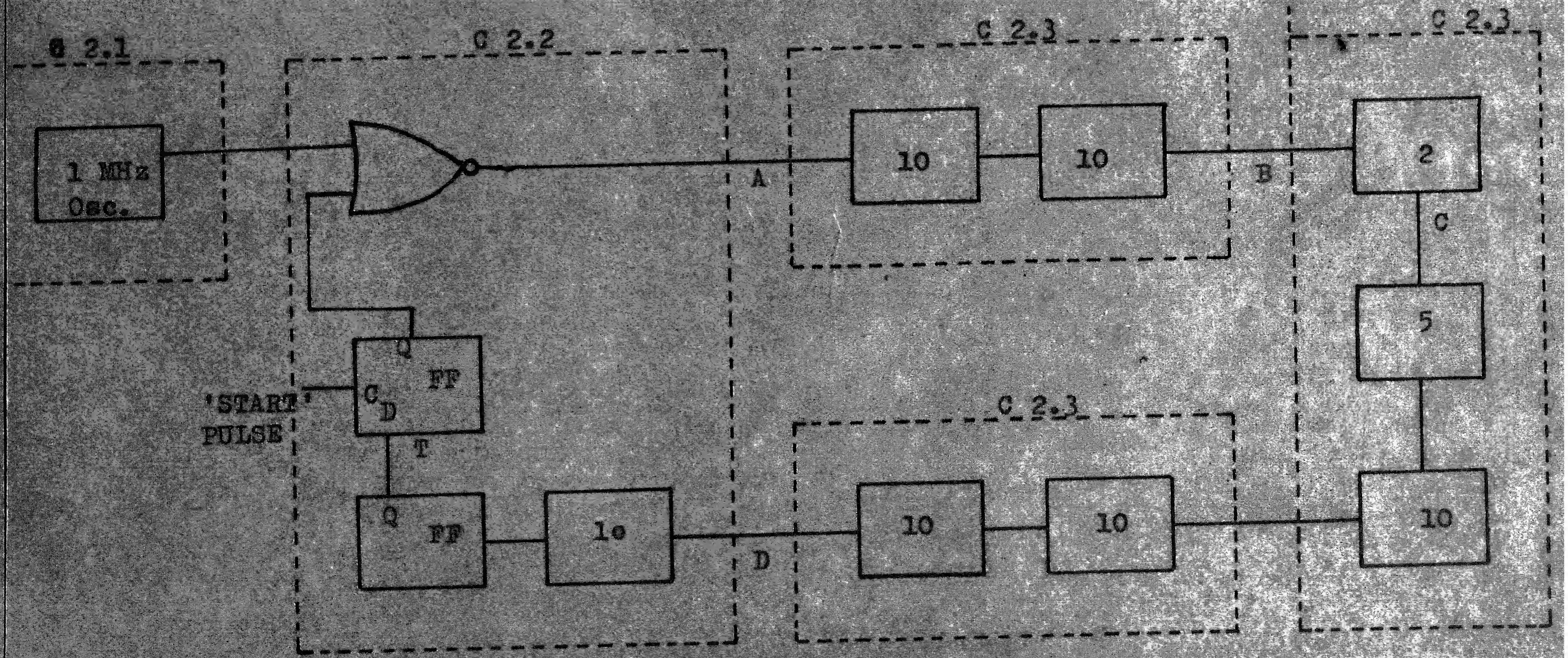


FIGURE 6.5 : LAY-OUT DIAGRAM OF THE DIGITAL CLOCK

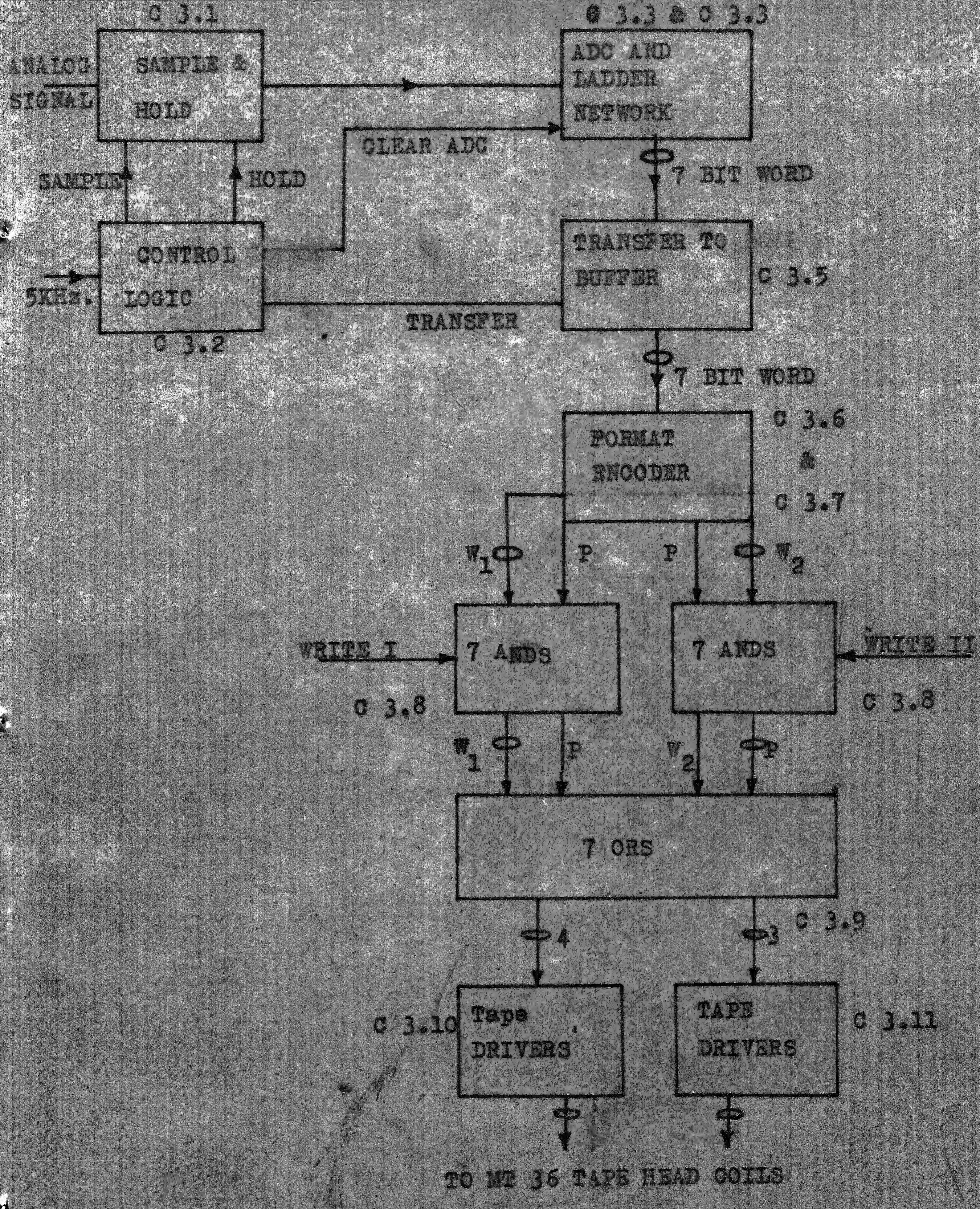


FIGURE 6.8 : CONFIGURATION OF CIRCUITS IN BIN'A'

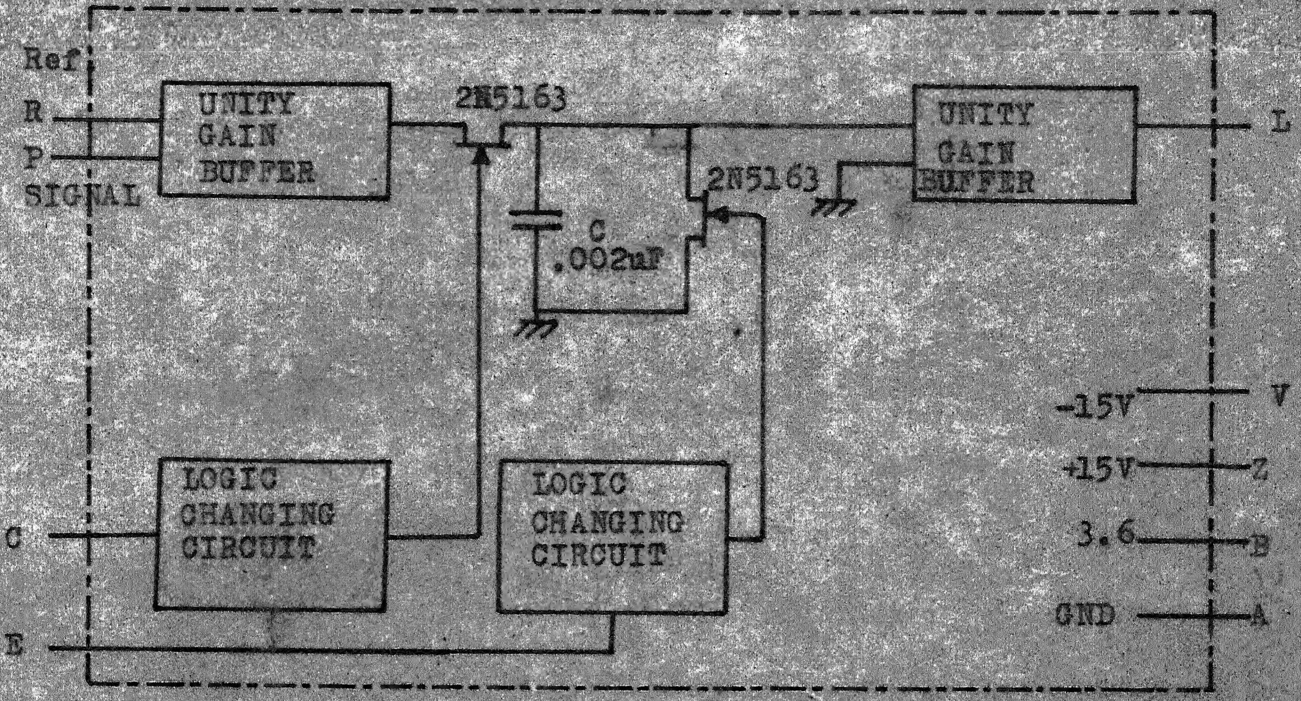


FIGURE 6.9 : SAMPLE AND HOLD CARD. C3.1

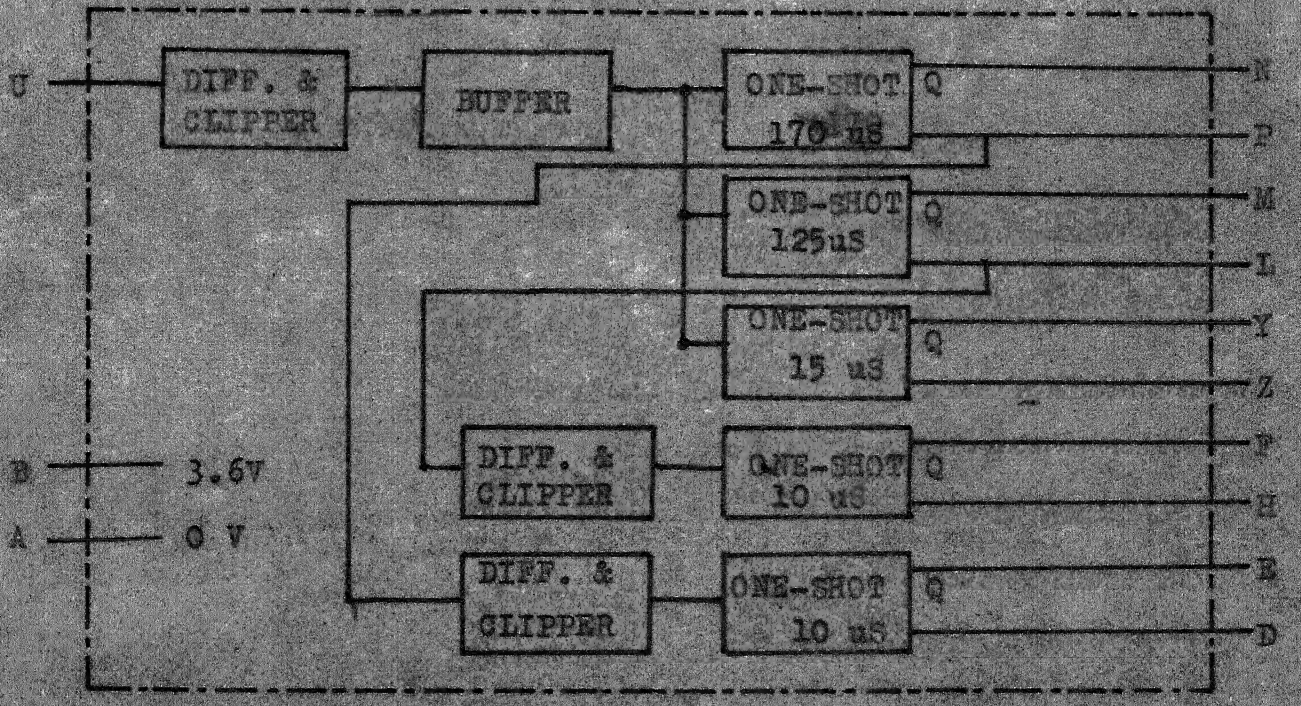
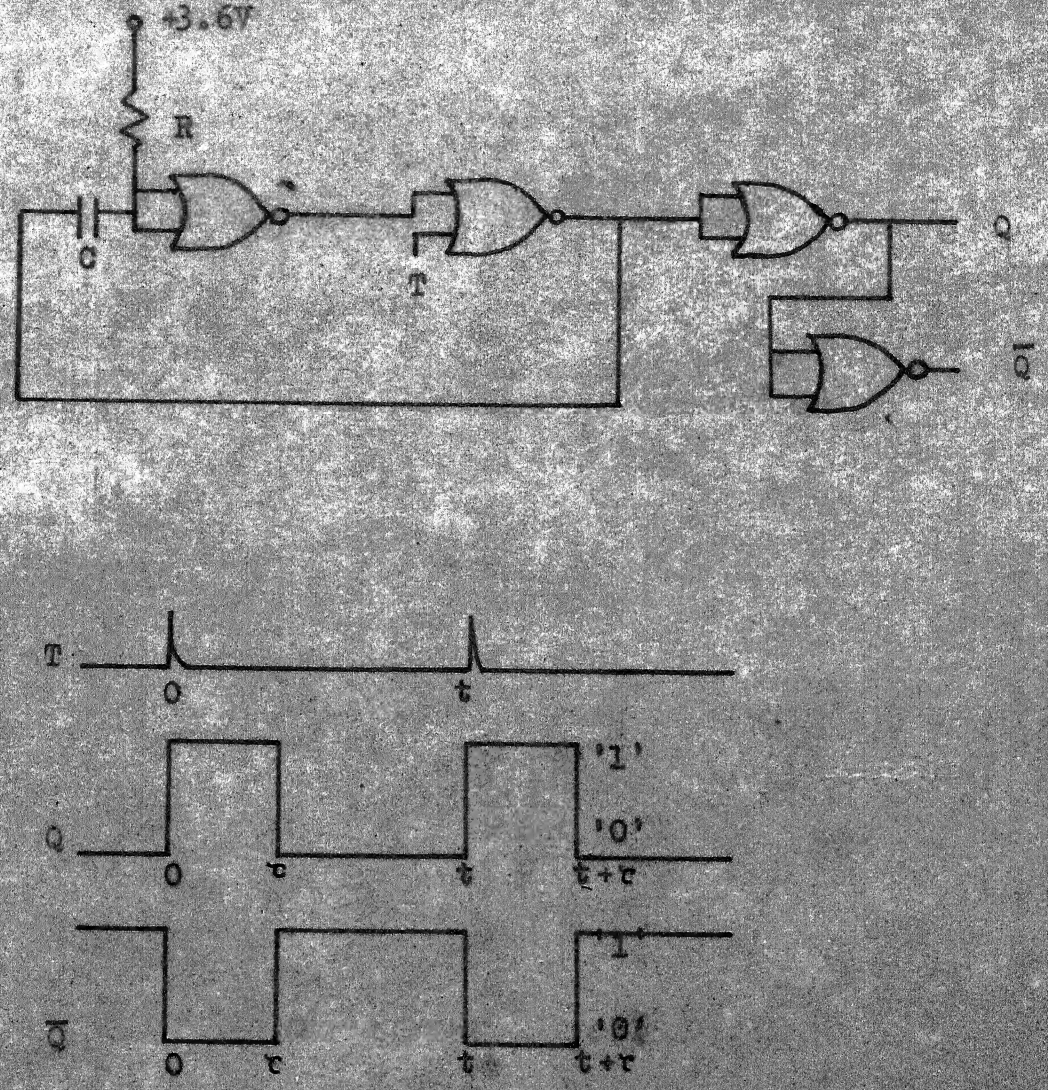


FIGURE 6.10 a : ONE-SHOTS FOR TIMING CONTROL



$\tau \doteq .3RC$

FIGURE 6.10 b : ONE SHOT REALIZATION WITH NOR GATES

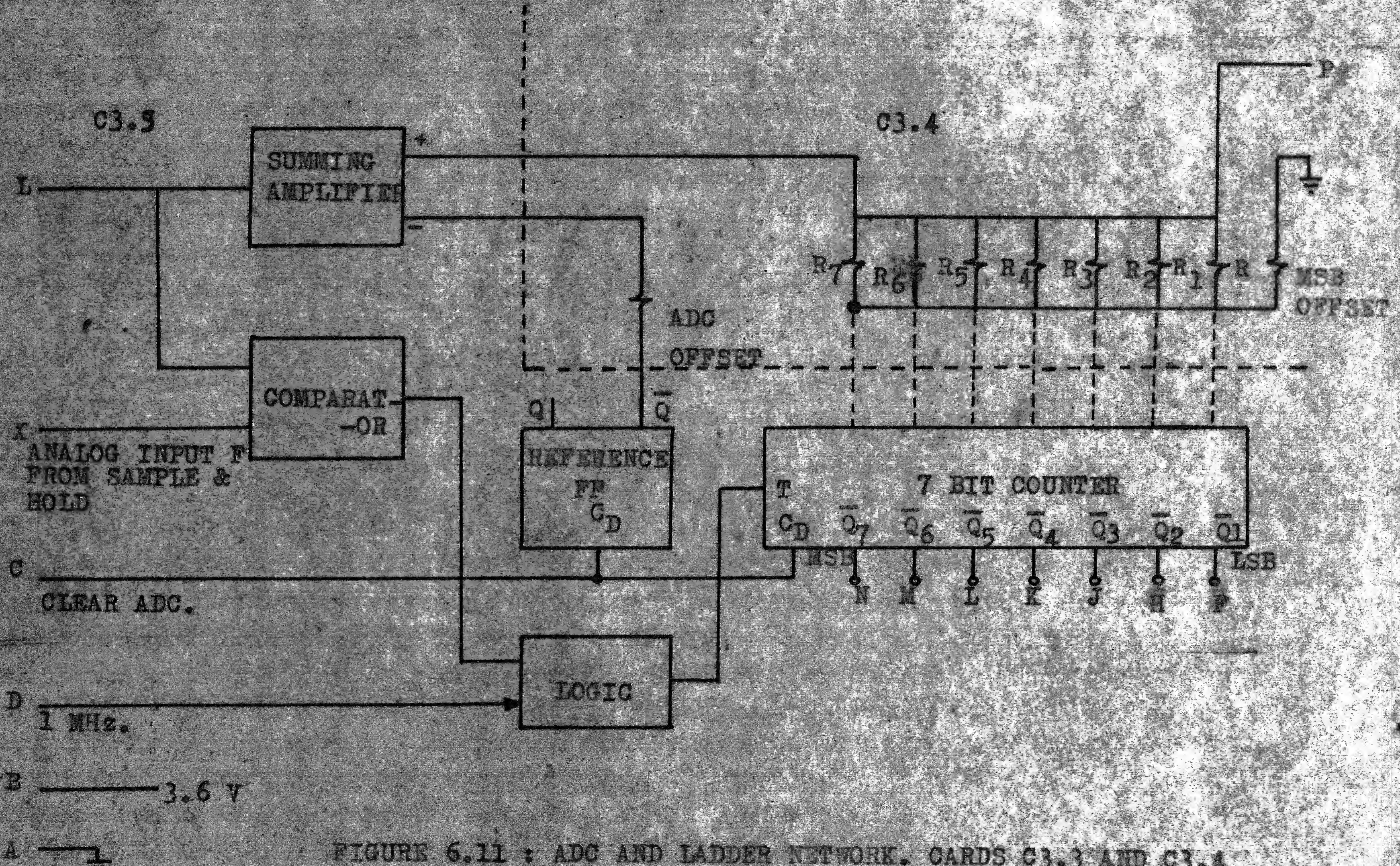


FIGURE 6.11 : ADC AND LADDER NETWORK. CARDS C3.3 AND C3.4

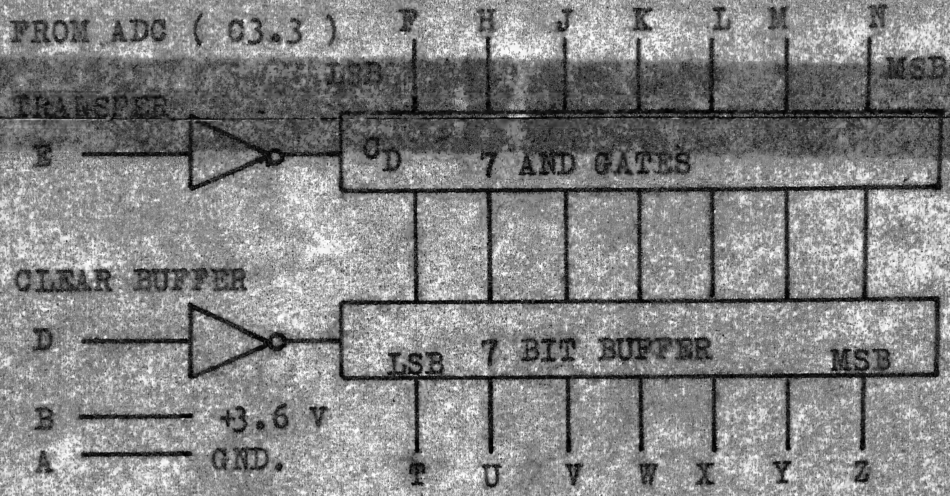


FIGURE 6.12 : TRANSFER TO BUFFER. CARD C3.5

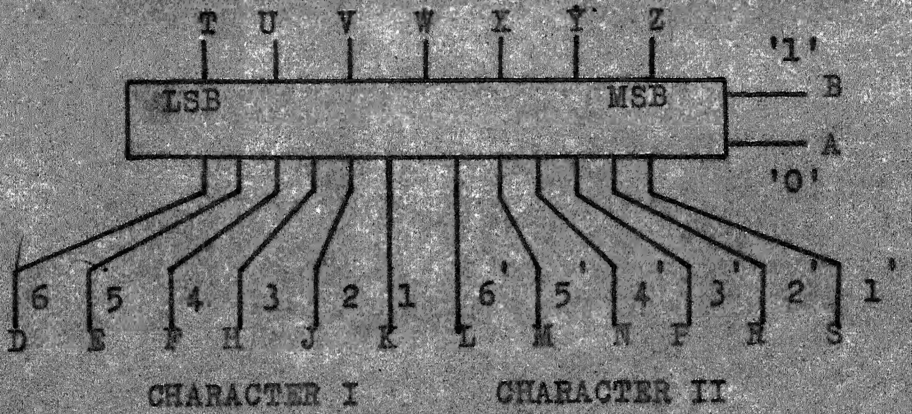


FIGURE 6.13 : PATCH UP CARD.cC 3.6

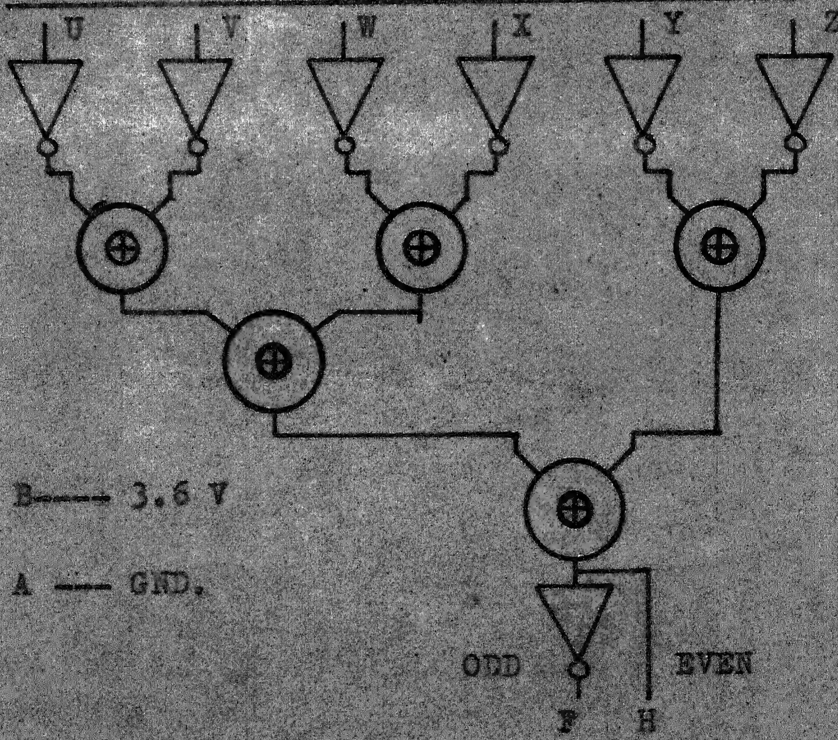
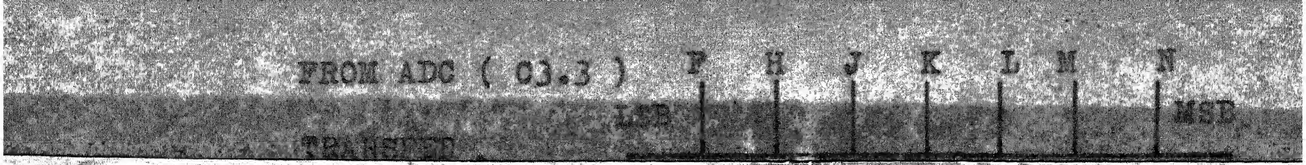


FIGURE 6.14 : PARITY CHECK CARD. C 3.7



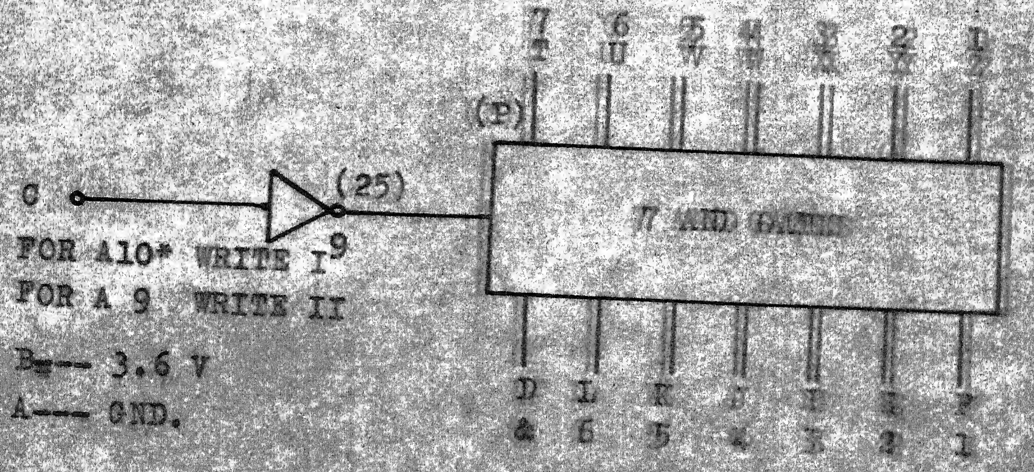


FIGURE 6.15 : SEVEN AND GATES. CARD C3.8

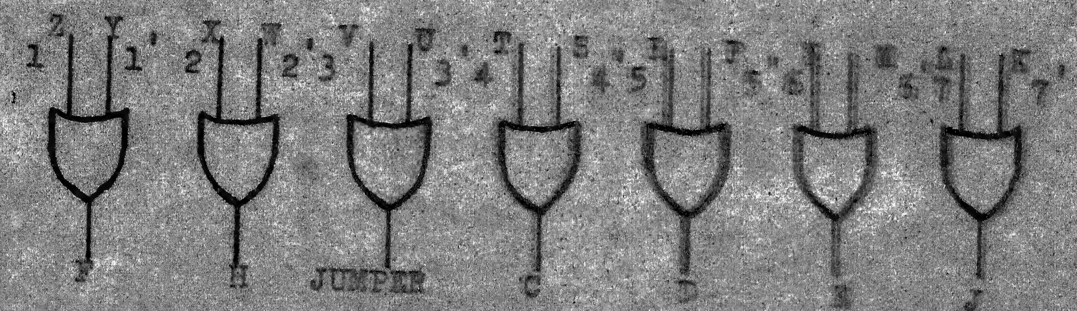


FIGURE 6.16 : SEVEN 'OR' GATES. CARD C3.9

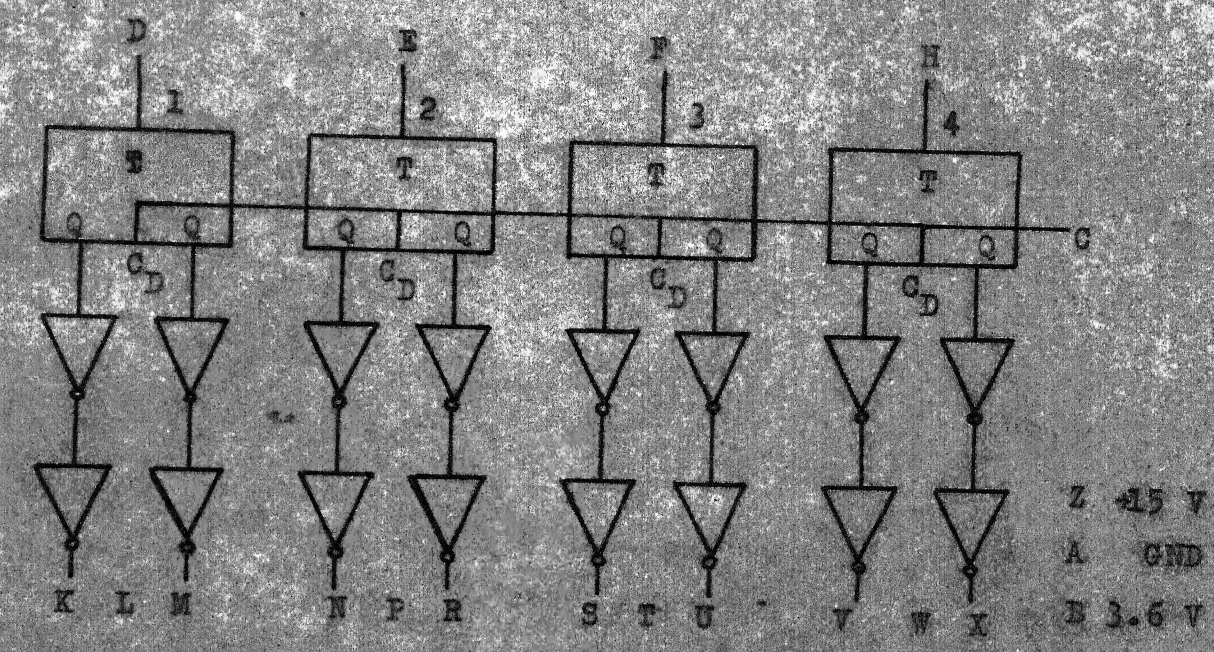


FIGURE 6.17 : FOUR TAPE DRIVERS. CARD C 3.10

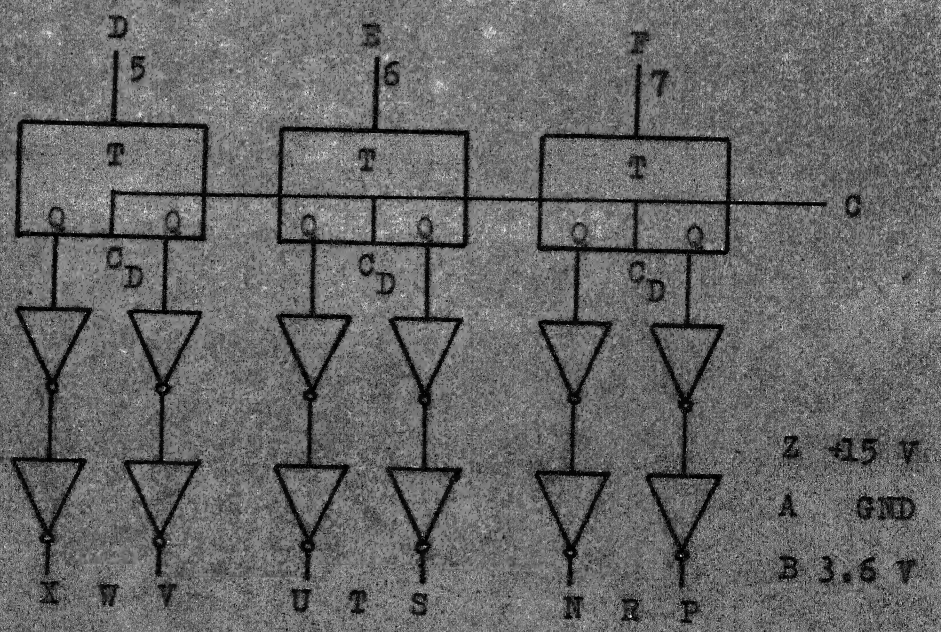


FIGURE 6.18 : THREE TAPE DRIVERS. CARD C 3.11

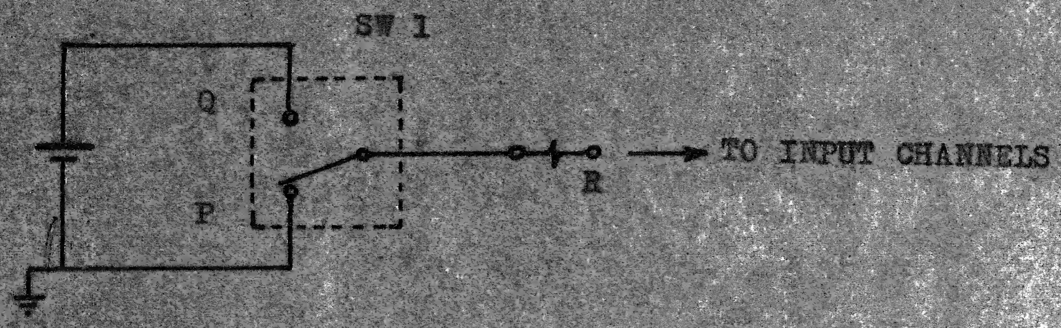


FIGURE 7.1 : INPUT SIMULATOR DIAGRAM FOR RECORD OSCILLATOR CALIBRATION